WWVB SYNCHRONIZED CLOCK

MODEL 8170

INSTRUCTION MANUAL

SPECTRACOM

Synchronizing Critical Operations™

www.spectracomcorp.com • sales@spectracomcorp.com
95 Methodist Hill Drive • Rochester, NY 14623 USA
Phone: +1.585.321.5800 • Fax: +1.585.321.5218

Manual Revision 1.0
0740-00000
Revision, if any, are located at back.
April 1988

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INSTALLATION & OPERATION

1.1 INTRODUCTION

The Spectracom Model 8170 NBS-Synchronized Clock is a WWVB receiver that decodes the time code signal and provides a front panel display of hours, minutes, and seconds. A serial RS-232C interface provides on command, day of the year, hours, minutes, seconds, time zone and status information. A 1.0-MHz signal phase locked to the WWVB carrier is provided on the rear panel along with a 1-Hz on-time pulse that signals the beginning of each second. A thumbwheel switch on the rear panel provides for time zone and path delay corrections.

1.2. INSTALLATION

1.2.1 UNPACKING

In the event of damage to the shipping carton or if there is hidden damage to the equipment, but the carton is not damaged, be sure to contact the carrier immediately so that his representative can witness any equipment damage that may exist inside the carton. If you fail to report shipping damage immediately you may forfeit any claim against the carrier. You should also notify SPECTRACOM CORPORATION of shipping damages so that we can assist you in obtaining a replacement or to repair the equipment.

Be sure to remove all items of equipment and accessories from the shipping carton before discarding it. This includes a three-conductor line cord and an instruction manual.

1.2.2 RESHIPMENT

If it is necessary to return the unit to the factory, the original shipping carton may be used. If it is not available, a carton of at least 250# test corrugated paper with at least two inches of polyethylene foam surrounding the unit must be used. The unit should be sealed in a plastic bag for moisture protection and a note must be included stating the reason for the return.

1.2.3 ANTENNA LOCATION

The antenna should be mounted a minimum of 25 feet from the receiver to prevent regeneration. The antenna MUST NOT be positioned next to the receiver or on top of it, making the results obtained with the equipment meaningless even though the green LOCK lamp on the receiver front panel may be lit.

The antenna must be as least three feet from any steel beams, roof decking, pipes, etc., as metal will detune the antenna and can cause as much as 20 dB degradation of the signal-to-noise ratio. The antenna must not be mounted under a metal roof or inside a building with heavy steel structural supports, as these shield the antenna from

the signal. Roof tops are generally good if a clear shot toward Fort Collins is available without being blocked by a large steel structure. Attics are ideal sites if the roof and rafters are not metallic. The signal-to-noise ratio will be optimized if the antenna is located as far as possible from local RF noise sources such as large electric motors, power lines, oscilloscopes, TV sets, or fluorescent or neon lamps that blink or sputter on and off. Any equipment containing a switching power supply is a probable cause of interference.

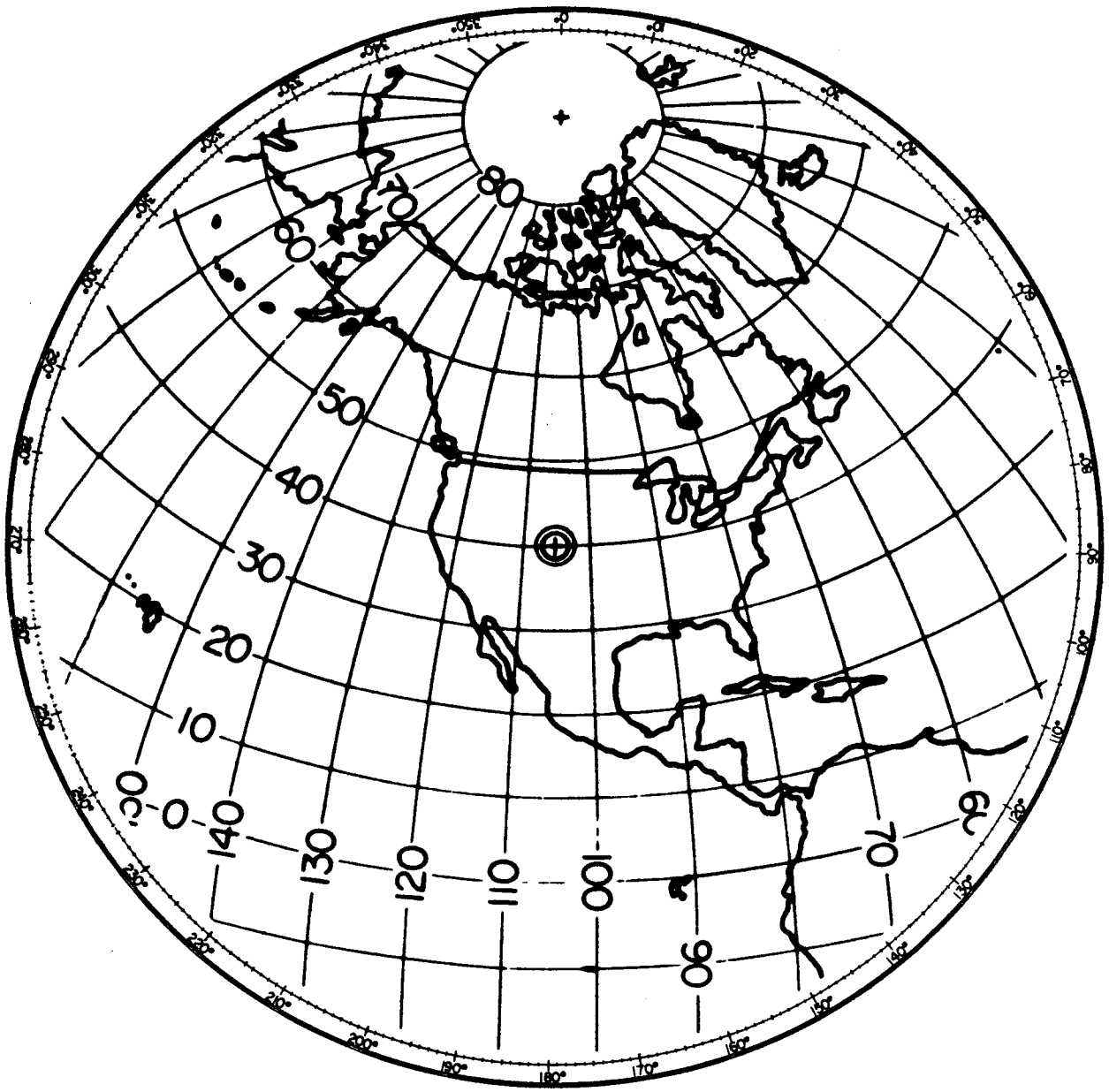
1.2.4 ANTENNA INSTALLATION

The antenna should be mounted where it will not be disturbed, supported by a non-metallic pipe such as a one-inch PVC water pipe. Holding the antenna two or three feet off the ground or rooftop is adequate in most cases. The tubular housing must be positioned broadside to Fort Collins, Colorado, where the transmitter is located (see Fig. 1-1, 1-2, 1-3), and horizontal to the ground, to allow maximum signal reception. No signal will be received if the tube points directly toward the transmitter site, as the antenna pattern nulls are located off the ends of the tube. The antenna position may be optimized using the signal strength measurement described in 1.3.3 SIGNAL STRENGTH.

When the lead-in coaxial cable (RG-58/U is recommended) is connected from the BNC connector on the antenna to the BNC conector on the receiver the system is ready for use, if the antenna has been installed and aimed properly. The antenna has a built-in preamplifier inside its housing that receives its DC operating voltage through the coaxial cable, therefore both the center conductor and the shield of the cable must be continuous from the antenna to the receiver. A short circuit in this line will not harm the equipment as the power supply is adequately protected.

1.2.5 INPUT POWER

The equipment may be operated from either 115 or 230 VAC $\pm$10%, 60-Hz line power. A slide switch on the rear panel selects either of the two line voltages. The receiver is shipped with the switch in the 115 VAC position, unless a tag is attached stating otherwise. If the line voltage switch is moved to select 230 VAC, the fuse must be changed also, as indicated on the rear panel. Before turning on the equipment after unpacking, make sure that this switch is in the correct position.



TO AIM ANTENNA AT FORT COLLINS, COLORADO, DETERMINE COMPASS HEADING FROM THIS MAP.

Draw a straight line from the receiver location through Fort Collins, Colo. at the center of the map. Continue until the line intersects the outer ring. The point at which the line intersects the outer ring indicates the compass heading for Fort Collins from your location.

FIG. 1-1 GREAT CIRCLE MAP CENTERED ON FORT COLLINS, COLORADO

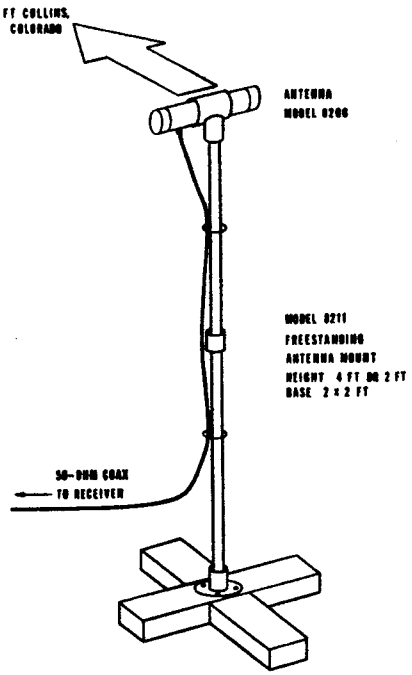


FIG. 1-2 ANTENNA MOUNT MODEL 8211

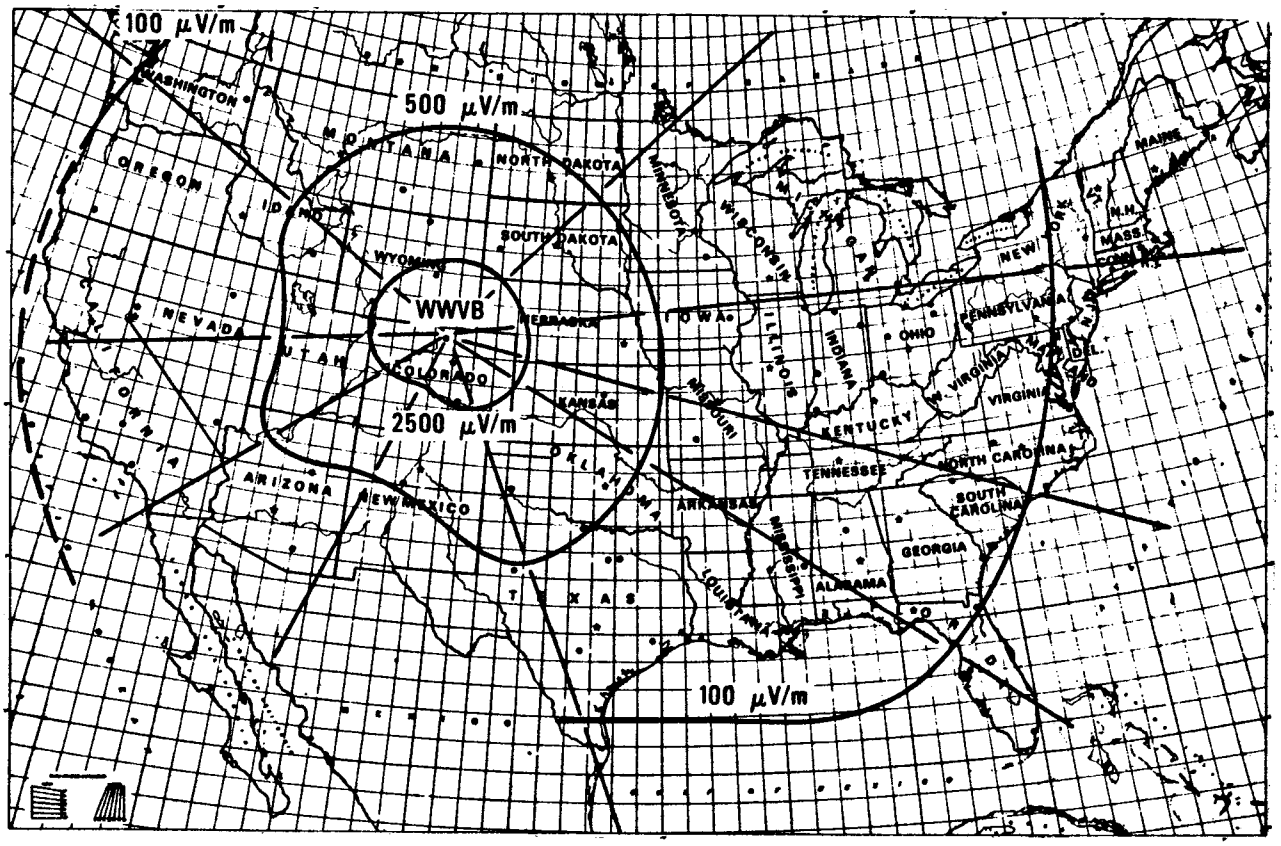


FIG. 1-3 SIGNAL STRENGTH MAP

1.2.6 OPERATING ENVIRONMENT

The equipment is designed for operation in a room temperature laboratory environment. Operation outside a temperature range of 0 to 50°C may cause malfunction or damage to the equipment.

1.2.7 BENCH OPERATION

The instrument is provided with four feet for standing on a benchtop surface, along with a tilt stand which may be used to provide a convenient viewing angle.

1.2.8 RACK MOUNT KIT (Option 01)

Units purchased with the rack mount kit are not provided with the tilt stand. The four mounting feet are included but these may be removed when the receiver is installed in a rack.

The rack mount panel extensions are installed by removing the vinyl-covered filler panels located just behind the handles on the sides of the enclosure. The rack mounting brackets are installed using the oval head #10-32 x 3/8 screws provided. Truss head #10-32 x 3/8 screws are furnished to mount the unit to the rack. (See Figure 1-4)

1.2.9 RACK MOUNT WITH SLIDES (Option 11)

The chassis section of the slides are attached to the sides of the receiver using the #10-32 x 3/4 screws provided. The filler plates are located between the slides and the receiver sides.

The stationary section of each rack slide must be assembled to the proper length for the rack being used, using the brackets, screws, and nuts provided. The slides are bolted to the front and rear channels of the rack using the #10-32 x 1/2 screws and nut plates as shown in Figure 1-5. Additional panel mounting angles (such as Emcor No. PMA) may be added to the rack cabinet for securing the front ends of the stationary slide sections if needed. They should be located immediately behind the panel mounting angles to which the equipment panel extensions will be fastened.

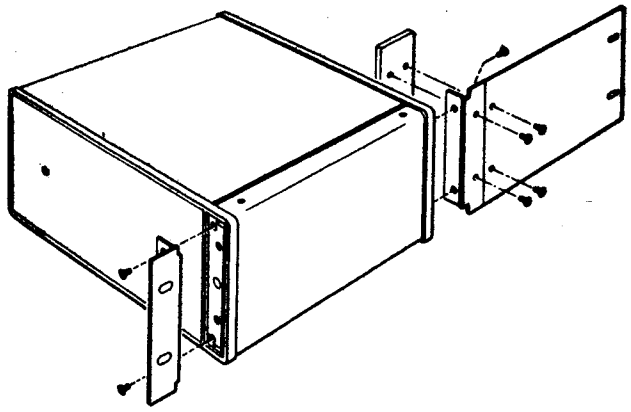
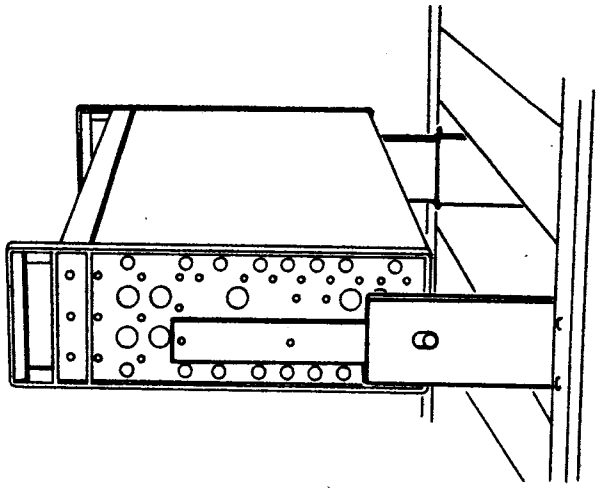


FIG. 1-4 RACK MOUNT OPTION 01



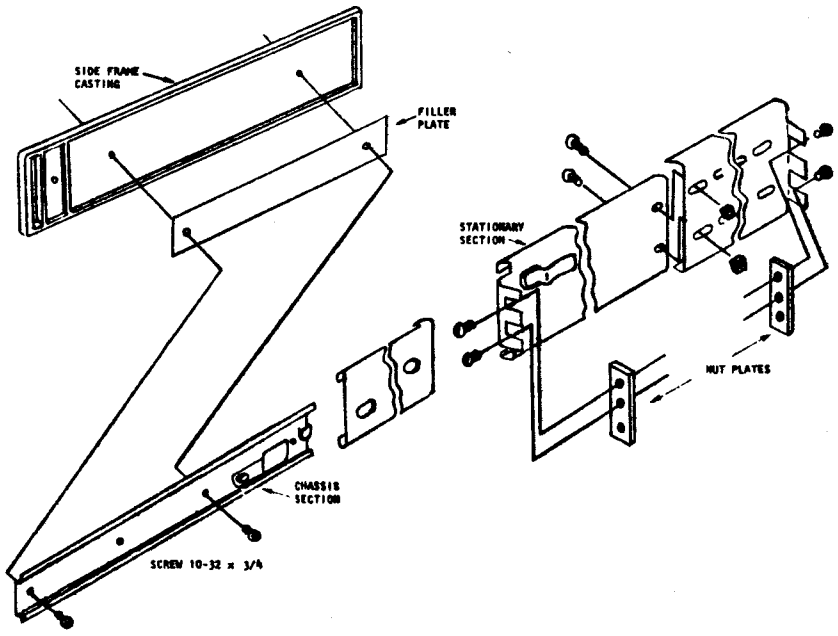


FIG. 1-5 RACK MOUNT WITH SLIDES (OPTION 11)

1.2.10 SELECTABLE BIT RATE

Switch (SW2) located on the microprocessor assembly A3 is a 10-position switch which controls the bit rate of the serial I/O port. The table below lists the bit rate as a function of the switch setting.

Switch Position	Bit Rate
0	75
1	150
2	300
3	600
4	1200
5	2400
6	4800
7	9600
8	19200
9	110

1.2.11 PREAMPLIFIER (Model 8207) INSTALLATION

The Spectracom Model 8207 Preamplifier is a low noise, tuned, 60 KHz line amplifier used in the antenna feed line wherever the WWVB signal strength is less than 50 uV/meter at the Model 8206 Loop Antenna or less than 0.3 uV at the receiver antenna terminal. Typical locations where the Preamplifier is probably required are Hawaii, Alaska, Puerto Rico, and the Canal Zone. The Model 8207 Preamplifier provides approximately 40 dB of gain between the antenna and receiver increasing sensitivity to 3.0 nanovolts.

The Preamplifier is connected in the antenna feed line with input connected to the antenna and output connected to the receiver. Because of the high gain of the system, it is recommended that the preamplifier be located at least 10 feet away from the receiver, perhaps where the antenna line enters the room from where the receiver is located. The antenna must be at least 25 feet beyond the Preamplifier from the Receiver. Switch A1S1 of the receiver RF Amplifier must be set at its right-hand position, marked PREAMP or P, prior to equipment turn-on, to apply DC voltage to the Model 8207 on the antenna feed line. If the preamplifier is removed from the system, the switch must be placed in the left-hand position, marked ANT or A prior to turn-on.

It is strongly recommended that no internal adjustment of the Preamplifier be made without consulting the factory.

1.2.12 MATING CONNECTORS

The mating connectors for the Remote Output, Parallel BCD, and RS-232C connectors on the rear panel are listed below.

REFERENCE	DESIGNATION	SPECTRACOM PART NO.	MFR. PART NO.	MFR
Remote Output	Plug, 9 position	J03309	205204-1	AMP
(Option 19)	*Socket Pins	P004001	1-66505-0	AMP
	Shell	H52090	206478-1	AMP
Parallel BCD	Plug, 50 position	J03350	205212-1	AMP
(Round Cable)	*Socket Pins	P004001	1-66505-0	AMP
	Shell	H52500	206478-5	AMP
(Flat Cable)	Plug, 50 position	-	609-50P	T&B ANSLEY
RS-232C	Plug, 25 position	J03325	205208-1	AMP
	*Socket Pins	P004001	1-66505-0	AMP
	Shell	H52250	206478-3	AMP

* The crimping tool for the pins is AMP 90302-1. The insertion/extractor tool is AMP 91067-2.

1.3 OPERATION

1.3.1 FRONT PANEL FUNCTIONS

Unlock/Lock Lamps: The red UNLOCK lamp is lit when there is insufficient signal received for the receiver to lock to the WWVB carrier. This is usually due to improper placement or aiming of the antenna. The green LOCK lamp lights when the receiver acquires phase lock.

Time Sync: The green lamp is turned on when the time code is fully decoded. In order to select the length of time before the time sync lamp goes out after loss of phase lock, switch (SW4-3,4) can be set to select 1 of 4 times:

SW4-4 Setting	SW4-3 Setting	Time (min)	Typical Error (msec)
0	0	10	1
0	1	20	10
1	0	60	30
1	1	180	100

The lamp will come back on after the receiver reacquires phase lock to the WWVB carrier and the time code is decoded.

If high accuracy during loss of signal is required then Option 24/25, TCXO and External Oscillator is recommended. Refer to Section 4 Options for details.

Display: The display initially indicates time since "power on" in the four right hand digits. After phase lock is achieved the sixth digit displays the code received. A zero (0) is a logical zero, a one (1) is a logical one, a two (2) is a position identifier and a four (4) indicates a bit error. After the code is successfully received universal coordinated time (UTC) minus the time zone switch setting is displayed.

1.3.2 REAR PANEL FUNCTIONS

Thumbwheel Switch: This is a 5-digit switch. The right two digits are TIME ZONE. The left three digits are PROPAGATION DELAY and RECEIVER DELAY inputs. The propagation delay can be calculated (see Section 1.3.9 PROPAGATION PATH DELAY). The receiver delay is a nominal 17 milliseconds. Set the switch to the sum of the path delay and receiver delay.

Daylight Savings Time: Use the TIME ZONE switch to adjust the display for local time.

Parallel BCD: Option 18 provides the day of the year, hours, minutes, seconds, time zone and status data on a 50-pin series D socket.

Remote Output Driver: Option 19 provides a RS-422 serial data output for driving Model 8172 Synchronized Wall Clocks or Model 8173 Multiple RS-232C Taps.

IRIG B Output: Option 23 provides 1-KHz carrier, amplitude modulated at 100 pps with time code or 100 pps DC level shift.

External Oscillator Input: Option 24 or 25, rear panel BNC input for 1.0-MHz standby clock oscillator.

1 KHz Output - Option 28, provides a 1-KHz signal phase locked to WWVB carrier. Brought out on pin 47 of 50-pin series D connector. Pin 50 is ground return.

Serial ASCII: This interface is a serial RS-232C port. The connector is a 25-pin series D socket.

There are 3 commands:
S - Set the clock
T - Read the time
D - Dump the memory

1 MHz: 1.0 MHz phase locked output. TTL compatible (SN74S140 source).

1 PPS ON-TIME: 1 pulse per second. TTL compatible (SN74S140 source). The leading edge is synchronized to the WWVB reduction of the carrier level that occurs at the beginning of every second.

Power: International Electrotechnical Commission (IECS) male line cord receptacle.

Line Fuse: AC line fuse. 3/4 ampere for 115 VAC operation and 3/8 ampere for 230 VAC operation.

Line Switch: Line switch to allow operation with 115 volt or 230 volt primary AC source.

Antenna: BNC connector for WWVB antenna.

1.3.3 SIGNAL STRENGTH

The Spectracom receiver may be used to measure relative field strength of the 60 KHz signal. This measurement may be used to optimize reception by indicating the best location and orientation of the antenna.

The WWVB receiver employs synchronous AGC which responds to the 60-KHz signal only and is not affected by noise. The AGC level, therefore, provides an excellent indication of signal strength.

To measure this AGC voltage, open the cover of the receiver and locate test points TP3 and TP6 on the Receiver board, A2. Place the positive lead of a DC voltmeter on TP6 (blue) and the negative lead on TP3 (orange). The input impedance of the voltmeter should be greater than 10 megohm. The voltage will be approximately 2.0 VDC at a field strength of 100 microvolts/meter using a properly oriented Model 8206 antenna. The AGC voltage will increase in strong signal locations, rising to a limiting value of approximately +3.6 volts as the front-end input signal level increases.

As the signal strength decreases to the receiver phase lock threshold of about 0.2 microvolts, the AGC voltage decreases to about +1.0 VDC. The red UNLOCK panel lamp will light below this level. The AGC voltage will decrease to a varying level around zero if the input signal is removed completely. As the signal is reapplied and increased, the receiver will again lock at an AGC level of approximately 1.0 volt.

The relative signal strength measurement may be used to aid antenna orientation by placing the antenna to maximize the AGC voltage measurement. The circuit that develops the AGC voltage has a very long time constant, so that a pause of 30 to 60 seconds is necessary

after each move of the antenna to allow the AGC to stabilize at the new level. A few minutes of experimentation should produce good antenna orientation.

1.3.4 INTERNAL SWITCHES

There are four, ten-pole BCD switch assemblies on the A3 Microprocessor board (014801).

The general purpose of these switches are as follows:

A3SW1 - Units-year select for option 30
A3SW2 - Selectable bit rate
A3SW3 - Tens-year select for option 30
A3SW5 - Code select switch - Position 1 selects IRIG B code. The remaining switches are reserved for future code options.

There is also a four-positon dip switch (A3SW4) and a one-position dip switch (A3SW6) on the A3 board.

The functions of these switches are as follows:

A3SW4 - The CF switch (SW4-1) controls data to/from the rear panel parallel BCD connector. This switch is functional when IRIG B Option 23 and Parallel BCD Option 18 are present. SW4-2 is the Option 30 select switch. SW4-3,4 controls Time Sync LED. See SW4 functions below.
A3SW6 - TTL/AM switch selects a TTL or amplitude modulated 1 KHz signal for the IRIG output.

The internal switches are set as indicated below when the unit is shipped from the factory, provided its corresponding option is present.

A3SW1	-	Present Unit's Year (Option 30)
SW2	-	2 (300 Baud)
SW3	-	Present Ten's Year (Option 30)
SW4-1	-	OFF (Option 18/23)
-2	-	OFF (Option 30 Enable)
-3,4	-	ON, ON (Time Sync Indicator)
SW5	-	1 (Option 23)
SW6	-	ON (Option 23)

If Option 23 is not available, SW5 and SW6 will not be on the board and SW4-1 will be non-functional.

The functions of SW2 and SW4 are listed below:

SW2 -	0	75 Baud Rate
	1	150
	2	300
	3	600
	4	1200
	5	2400
	6	4800
	7	9600
	8	19200
	9	110

SW4 - 1 Control Function for Option 18/23
ON - Data read into 8170
OFF - Parallel BCD time of year data is from 8170

- 2 Option 30 Select
OFF - STD output
ON Option 30 Fully Decoded Text Stream

SW4-3,4 Time Sync LED Indicator: See Table Below

4	3	TIME (min)	ERROR (msec)
0	0	10	1
0	1	20	10
1	0	60	30
1	1	180	100

(0 = OFF; 1 - ON)

1.3.5 INITIAL TURN-ON

After the receiver and antenna have been installed, plug the receiver into the power line, after making sure that the rear panel slide switch is in the correct position for the line voltage. Note that the green LOCK lamp lights within one minute. If the red UNLOCK lamp stays lit, insufficient signal is being received, probably due to improper antenna placement or alignment. The time since turn-on is displayed in minutes and seconds. The time code received is displayed in the left digit.

The time code display is coded:

0 - binary zero
1 - binary one
2 - position identifier
4 - bit error

The clock receives the code and sets itself automatically. The time it takes to set is dependent on the quality of the signal received. The quality of the signal is indicated by the code received. If many 4's are displayed, then the signal is poor. If the

signal is good, then the clock will set in a few minutes. If there is a weak or noisy signal, it will take longer to set.

1.3.6 COMMANDS

Commands are accepted through the Serial ASCII port. Commands are:

T - print the Time
S - Set the time
D - Dump the memory

Serial Data Interface:

RS-232 Port: Standard in all units, provides day and time in response to a T input command. S command allows operator to set clock via a data terminal keyboard. D command causes a memory dump of statistical data for performance evaluation. A character consists of 1 start, 8 data, and 2 stop bits. Data rate is selectable from 300 to 19,200 baud.

Serial Data Structure: Response to a T command is:

(CR)(LF)I(SPACE)(SPACE)DDD(SPACE)HH:MM:SS(SPACE)(SPACE)TZ=XX(CR)(LF)

where:

I = space if clock set by WWVB (TIME SYNC lamp on)
    * if clock set manually via RS-232 port
    ? if time sync lamp is off
DDD = day of the year
HH:MM:SS = hours:minutes:seconds
XX = time zone switch setting at rear panel
Output is in UTC minus the time zone switch setting.

Option 30 Fully Decoded Text Stream: This alternate data format can be furnished when the unit is purchased:

(CR)(LF)I(SPACE)WWW(SPACE)DDMMMYY(SPACE)HH:MM:SS(CR)(LF)

where: I = as defined above
WWW =day of week (MON, TUE, WED, etc.)
DD = numeric day of month (1 to 31, leading zero suppressed)
MMM = month (JAN, FEB, MAR, APR, etc.)
YY = year without century (83, 84, 85, etc.)
HH:MM:SS = as defined above.

"S" Command - to manually set the clock, enter:

SDDDHHMMSS

where: S = set command
DDD = UTC day of year
HH = UTC hours
MM = minutes
SS = seconds

Entry of the last seconds digit sets the clock to UTC time minus the time zone switch settings. The WWVB-derived on-time pulse increments the clock every second. If phase lock to the carrier has been acquired, the on-time second pulses are phase locked to the time code pulses even though the unit may temporarily be unable to decode the incoming signal. Thus, if the manual setting started the clock within one second after the correct on-time pulse, it will run truly on-time, as though it had set itself.

If Option 30 is present and the operator enters 366 for DDD day and the internal year switch is not set to a leap year, then the error message "*CHK YEAR SW" will be printed.

"D" Command - the "dump the memory" command, will print the contents of the 256-byte RAM memory. Performance event counters stored in RAM are:

Phase Lock Lost Counter	PLLC
Time Code Compare Counter	TCCC

The print out represents physical address locations 0800 through 08FF. The data is printed in hexadecimal notation. PLLC is a two-byte counter whose contents are printed at row 0810, columns 8 and 9. The first byte is the least significant byte. The counter records the number of times phase lock has been lost since power-on.

The Time Code Compare Counter, TCCC, records the number of times the received data compares with the expected value. It is printed at row 0820, columns 8 and 9. It is a 2-byte hexadecimal number printed least significant byte first.

Figure 1-6 is the print-out from a sample dump command.

1.3.7 PHASE ADJUST TABLE

The 1 PPS on-time pulse is phase locked to the leading edge of the received time code signal. After the initial turn-on sequence the phase adjustments are in 0.1 millisecond increments. Each time an adjustment is made the time and direction of the adjustment are logged in a circular table. The table is located at 08A0 through 08DE. The table contains the data on the last 21 phase adjustments. UTC hours and minutes followed by 00 or FF are logged, where 00 indicates the 1

PPS was shifted 0.1 millisecond left (early) and FF indicates that the 1 PPS was shifted 0.1 millisecond right (late). The current position pointer is located at row 0800, columns D and E, least significant byte first. This points to the memory location where the next adjustment will be stored.

After the unit has been on a few days the adjustment interval will exceed 24 hours. If adjustment data is desired the memory should be dumped at least once every 24 hours. This eliminates ambiguity concerning which day the adjustment was made.

1.3.8 TIME FLAGS

At power-on or after the signal has been lost for longer than 60 minutes (depending on SW4-3,4) the Time Sync light will be off. This indicates that the time may be in error by greater than 30 milliseconds. If high accuracy during loss of signal is required, then Option 24/25, TCXO and External oscillator is recommended. See Section 4 Options for details. The Time Sync light is turned on when a good time code is received. A received time code must pass a number of tests. When the seconds, minutes, hours and days portion of the time code are acceptable, flags are set to FF at row 0880, columns 8 through C. The clock is set and the Time Sync light is turned on when all the flags are set. This data is useful during the initial installation and trouble shooting to determine the progress of the self-setting process.

Once the Time Sync light is on the clock will keep UTC time. The display will be changed when 3 consecutive good compares are received that do not agree with the display data. This will happen when the leap second is inserted.

1.3.9 TIME CODE FORMAT

The WWVB time code is generated at the transmitter by a reduction of the carrier power of 10 dB at the beginning of each second. It is restored to a full power 200 milliseconds later for a binary zero, 500 milliseconds later for a binary one, and 800 milliseconds later for a position identifier. Decoding a one-minute data stream yields day of the year, time of day, and a correction factor for converting from atomic time (Coordinated Universal time, UTC) to earth time (UTI). Figure 1-7 WWVB TIME CODE FORMAT shows the coded data in a 1-minute time frame.

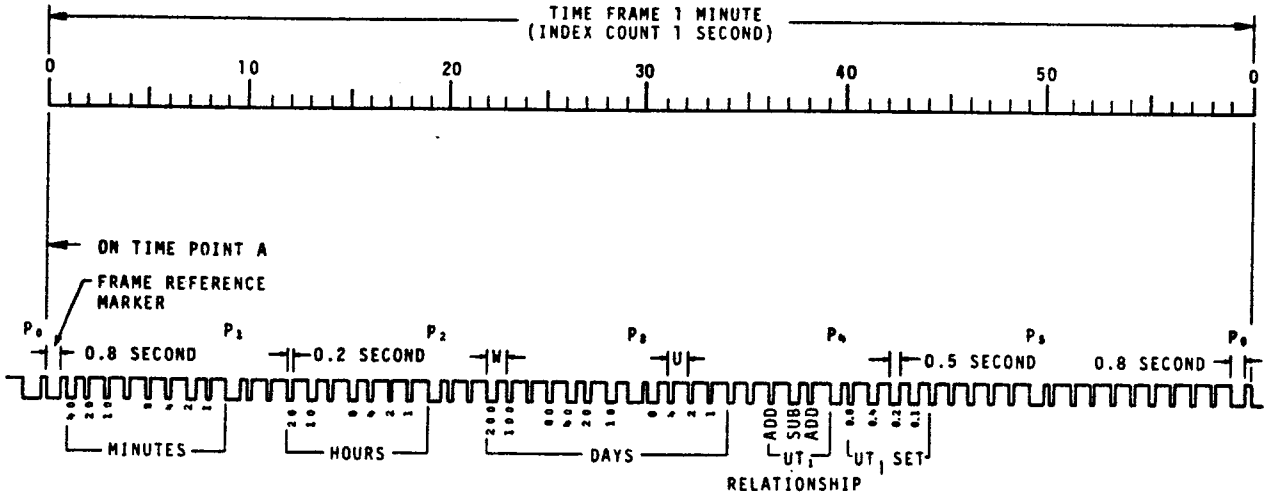
PLLC

TCCC

Pointer to phase adjust table

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0800	D0	48	00	1D	02	D0	E9	F4	00	10	00	FF	14	A3	08	FF	
0810	00	FF	00	01	00	00	F4	00	00	00	45	54	00	FF	00	00	
0820	00	27	28	14	25	05	00	01	99	02	01	00	00	00	99	49	
0830	29	28	14	25	00	00	00	03	01	28	FF	34	48	00	00	00	
0840	42	31	28	14	02	50	50	00	00	32	28	14	25	05	00	00	
0850	30	30	20	20	20	32	35	30	20	31	34	3A	32	38	3A	32	
0860	33	20	20	54	5A	3D	30	30	0D	0A	00	00	53	48	00	00	
0870	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	
0880	80	48	7D	00	0C	44	00	00	FF	FF	FF	FF	00	00	00	00	Time Flags
0890	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	
08A0	06	13	00	15	20	00	15	50	FF	19	04	FF	22	00	FF	00	
08B0	00	FF	01	53	00	02	15	00	02	46	00	03	13	00	03	54	Phase Adjust Table
08C0	00	04	48	00	09	51	00	10	39	00	11	12	00	14	39	FF	
08D0	17	03	FF	20	35	FF	04	25	00	09	12	00	20	52	FF	00	
08E0	00	00	00	00	00	00	00	00	00	03	43	B4	45	EA	47	F2	
08F0	41	88	47	00	49	00	00	00	00	54	64	04	41	00	00	00	

FIG. 1-6 SAMPLE MEMORY DUMP



BINARY CODED DECIMAL TIME-OF-YEAR CODE WORD (23 DIGITS)
CONTROL FUNCTIONS (15 DIGITS) USED FOR UT_1 CORRECTIONS
6 PPM POSITION IDENTIFIER MARKERS AND PULSES (P_0 THRU P_5)
(REDUCED CARRIER 0.8 SECOND DURATION PLUS 0.2 SECOND DURATION PULSE)
W - WEIGHTED CODE DIGIT (CARRIER RESTORED IN 0.5 SECOND - BINARY ONE)
U - UNWEIGHTED CODE DIGIT (CARRIER RESTORED IN 0.2 SECOND - BINARY ZERO)

NOTE: BEGINNING OF PULSE IS REPRESENTED BY NEGATIVE - GOING EDGE.

UTC AT POINT A	UT1 AT POINT A
258 DAYS	258 DAYS
18 HOURS	18 HOURS
42 MINUTES	41 MINUTES
	59.3 SECONDS

FIG. 1-7 WWVB TIME CODE FORMAT

1.3.10 PROPAGATION PATH DELAY

Radio waves at low frequencies use the earth and the ionosphere as a waveguide and follow the earth's curvature for long distances. To compute the propagation path delay the great circle distance between the two points is divided by the speed of light.

The approximate formula for finding the great circle distance from Ft. Collins, Colorado, to another point in the northern hemisphere is given below. The error is 2% or less.

The Great Circle Map shown in Figure 1-1 may be used to determine the approximate receiver location.

$$\text{Distance} = 60 \cos^{-1} (.758 \cos (\text{LAT}) \cos (\text{P}) + .652 \sin (\text{LAT}))$$

nautical miles.

where: LAT = latitude of receiver
P = Longitude of WWVB minus the longitude of receiver
WWVB is at 10502' 39.5" W longitude
The speed of light is 300 Km/millisecond

To convert from nautical miles to millisecond delay:

$$\text{PATH DELAY} = \frac{\text{Nautical Miles} \times 1.8522 \text{ Km/Nautical mile}}{300 \text{ Km/msec}}$$

An example of the calculation is given below for Boston:

$$\text{PATH DELAY} = \frac{1521 \text{ nautical miles} \times 1.8522 \text{ Km/nautical mile}}{300 \text{ Km/msec}}$$

$$= 9.4 \text{ milliseconds}$$

The path delay from the WWVB transmitter in Ft. Collins, Colorado, to Boston is 9.4 milliseconds.

Figure 1-8 Path Delay Map shows the United States with concentric circles around Ft. Collins, Colorado. The radius of the inner circle is 600 Km and represents a 2 millisecond path delay. Outer circles represent increasing 2 millisecond delays. The map provides only an approximate value for path delay.

Add the calculated path delay to the 17 millisecond receiver delay and enter the sum into the path delay thumbwheel switch.

1.3.11 TIME ZONE SETTINGS

The time zone switch is used to offset UTC time to display and output a local time. Once a time zone is entered the Model 8170 will reflect the local time within one second.

Use the table below to determine time zone settings. Areas that do not observe daylight savings time should enter the standard time value for that time zone.

	TIME ZONE SETTING	
TIME ZONE	STANDARD TIME (OCTOBER - APRIL)	DAYLIGHT SAVINGS TIME (APRIL - OCTOBER)
ATLANTIC	4	3
EASTERN	5	4
CENTRAL	6	5
MOUNTAIN	7	6
PACIFIC	8	7
UTC	0	0

TABLE 1-1 TIME ZONE SETTINGS

The time zone switch must be manually updated when changing from standard time to daylight savings time and back to standard time.

1.3.12 LEAP YEAR SWITCH

The 365/366 toggle switch must be placed in the 366 position during leap years. This allows the receiver to automatically convert day-of-year properly to month and day during leap years. This also allows receivers that convert UTC time to local time to "back up" properly to either day 365 or 366 as appropriate upon change of year.

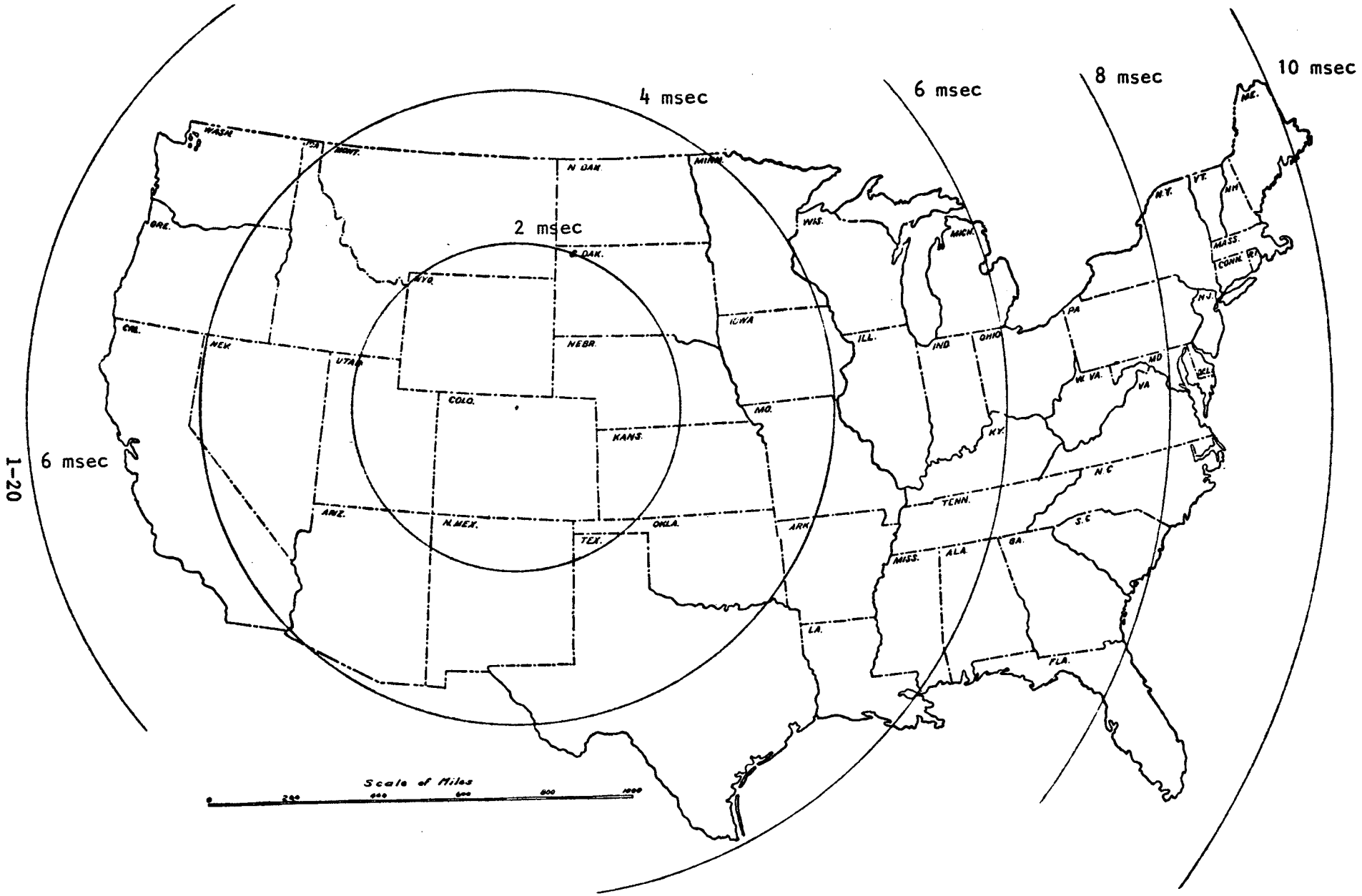
1.3.13 SPECIFICATIONS

RECEIVER:

Received Standard Frequency: 60 KHz NBS Station WWVB

Sensitivity: 0.4 uV rms into 50 ohms. Minimum field strength at antenna, 25 uV per meter when used with Model 8206 Antenna. 40 dB additional gain may be obtained using Model 8207 Preamplifier in remote locations such as Hawaii, Puerto Rico, Panama, and Alaska.

Receiver Delay: nominal 17 milliseconds. The precise calibration of receiver delay and propagation delay may be made with a portable clock.



1-20

FIG. 1-8 PATH DELAY MAP

Phase Lock Indication: Red/Green UNLOCK and LOCK lamps on front panel show synchronous detection of WWVB carrier signal.

SIGNAL OUTPUTS

1 MHz: Standard frequency output phase locked to WWVB carrier. A 3.4 volt TTL compatible square wave into an open circuit. A 2.0 volt square wave into 100 ohms.

1 PPS: A Positive-going "on-time" signal phase locked to the leading edge of the WWVB 10 dB power reduction. A 3.4 volt TTL compatible pulse (10% duty cycle) into an open circuit. A 2.8 volt pulse into 100 ohms.

SERIAL ASCII: An Intel 8251A Programmable Communication Interface is used to provide the RS-232 informaton. It is programmed for:

1 start bit
8 bits per character
2 stop bits

The Serial ASCII port provides the day and time data in ASCII format. The interface is RS-232C compatible. The connector is a 25-pin series D female connector DB-25S or equivalent. The signal names and pin numbers are listed below:

SIGNAL	MNEMONIC	PIN
Protective Ground	AA	J5-1
Transmit Data	BA	J5-2
Receive Data	BB	J5-3
Request to Send	CA	J5-4
Clear to Send	CB	J5-5
Data Set Ready	CC	J5-6
Signal Ground	AB	J5-7
Received Line Signal Detector	CF	J5-8

The Request to Send and Clear to Send signals are connected together inside the Model 8170. The Received Line Signal Detector and Data Set Ready will be high when power is on. They are connected together and tied to +12 volts through a 5.1K resistor inside the Model 8170.

The time data is sent out in reponse to a "T" command. The data represents the time at the beginning of the first character sent. If Option 30 is present the date will be sent as well as the time data. The baud rate is selected by A3SW2.

Relative to RS-232C definitions, the Model 8170 is a data communication equipment DCE. Transmit Data, BA, is TO the Model 8170. Received Data, BB is FROM the Model 8170.

SELECTABLE BIT RATE The Serial ASCII output is internally switch-selectable to 75, 150, 300, 600, 1200, 2400, 9600, 19,200, and 110 bits per second by switch A3SW2.

MECHANICAL & INSTALLATION

Size: 5.25H x 13.5D x 17W (inches). Height is 6 inches including feet. If feet are removed, unit may be mounted in a 5 1/4" rack space.

133 H x 343 D x 432 W (mm). Height is 152mm including feet. Handles protrude 1.75 inches (45mm) from front panel. Allow 2-3 inches cable clearance at rear.

Weight: 15 lbs. (6.7 Kg): Shipping Wt. 18 lbs. (8.2 Kg).
Line Power: 115/230 VAC +-10%, 50/60 Hz, 20 VA

Operating Temperature: 0 to 50C.

OPTIONS AND ACCESSORIES AND RELATED UNITS

Options:

Option 01: Rack Mount Kit
Option 11: Rack Mount with Slides
Option 15: Timing Pulse Outputs
Option 18: Parallel BCD
Option 19: Remote Output Driver is now standard on units with S/N 8170-601 and higher.
Option 23: IRIG B Output
Option 24: TCXO
Option 25: External Oscillator Input
Option 28: 1 KHz Output
Option 30: Fully Decoded Text Stream

Accessories:

Model 8206 Loop Antenna
Model 8207 Line Preamp (60 KHz)
Model 8211 Antenna Mount

Related Products

Model 8172 Remote Clock
Model 8173 Multiple RS-232 Tap

SECTION 2

8170

THEORY OF OPERATION

2.1 INTRODUCTION

The 8170 consists of an RF Amplifier Assembly, a Receiver Assembly, a Microprocessor Assembly and a Display Assembly as shown in Figure 2-2 Receiver Block Diagram, and Figure 2-3, Microprocessor Block Diagram.

The 60 KHz output of the RF Amplifier is fed to the receiver assembly where the carrier is detected and translated to a phase-locked 10 MHz. This is divided down to provide a 1-MHz NBS phase-locked signal at the rear panel. The AGC voltage is generated in the Receiver Assembly for use in controlling the gain of the RF Amplifier.

The time code information is detected and sent to the Microprocessor Assembly along with the phase lock/unlock condition.

The Microprocessor Assembly consists of an 8085A microprocessor, 6K of EPROM, 512 bytes of RAM, 2 timer chips, a priority interrupt controller, a USART and LED display interface.

The processor integrates out the noise, measures the pulse width, decodes the signal, phase locks a 1-Hz on-time pulse to the received signal, and controls the display and time-of-year outputs.

Input signals from the thumbwheel switch on the rear panel provide time zone and path delay corrections.

2.2 MAINFRAME SCHEMATIC

Figure 2-1 Mainframe Schematic shows the interconnection between the various subassemblies. Each of the boards are described in this section.

2.3 A1, RF AMPLIFIER, P/N 001100

The RF Amplifier assembly filters and amplifies the antenna signal to a level suitable for use by the A2 Receiver Assembly. (See Figure 2-4 for the schematic.)

The signal from the antenna is applied to input transformer T1 which matches the 50-ohm line impedance to the input of the first stage of amplification, Q1. The impedance looking into transformer T1 is approximately 50-ohms, with the secondary of T1 and capacitor C2 forming a 60-KHz tuned circuit with approximately a 200-Hz bandwidth. The output of amplifier Q1 is applied to transistor Q2 which, together with crystal Y1 and capacitors C7, C8, C9 and C10, form a narrow bandpass crystal filter centered at 60 KHz. Capacitors C9 and C10 feed to the output side of the crystal a signal that is 180° out of phase and is tuned so that a passband null occurs at 100 KHz. This combination provides a sharp bandpass response at 60 KHz with very steep high frequency rejection.

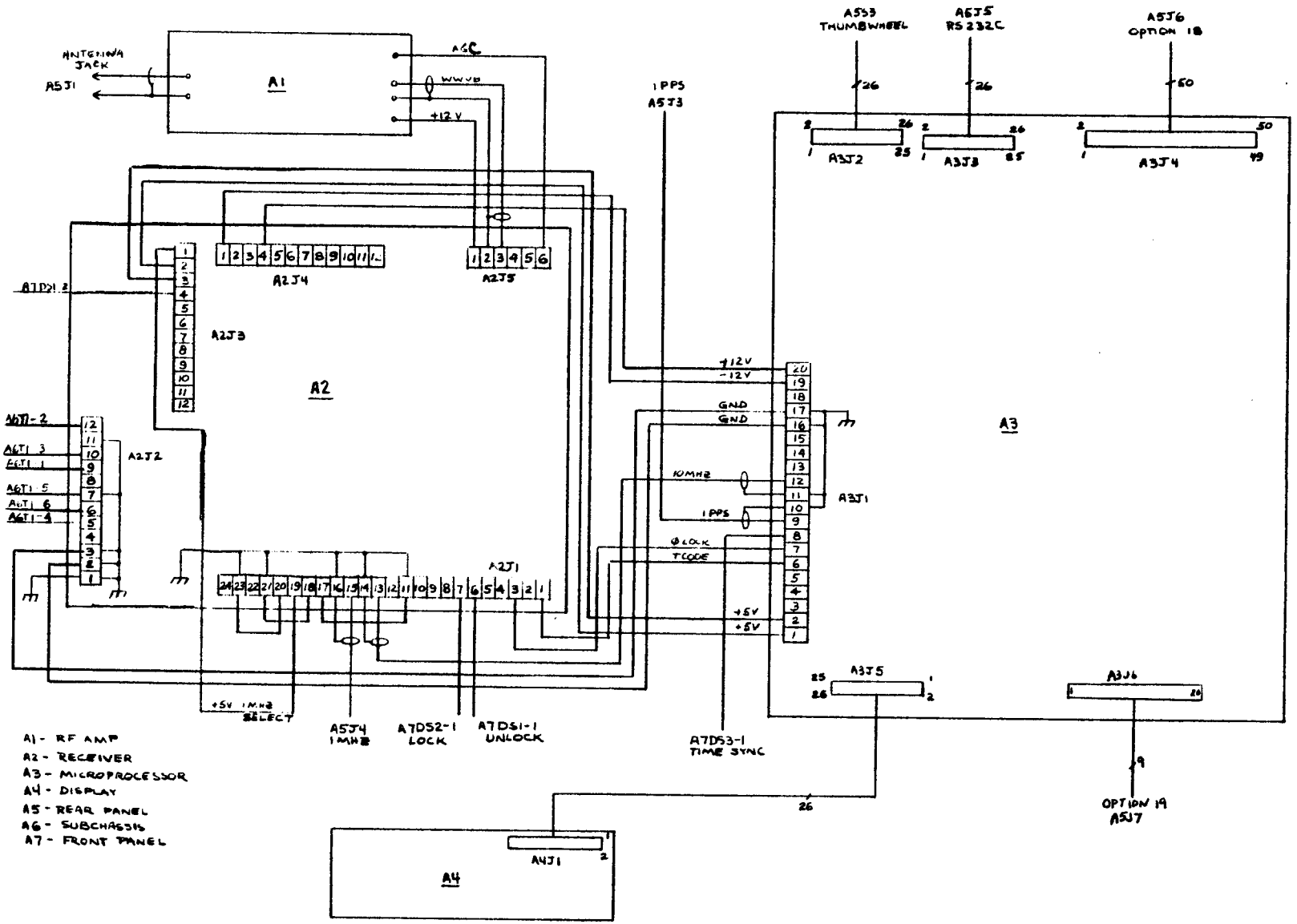


FIG. 2-1 MAINFRAME SCHEMATIC

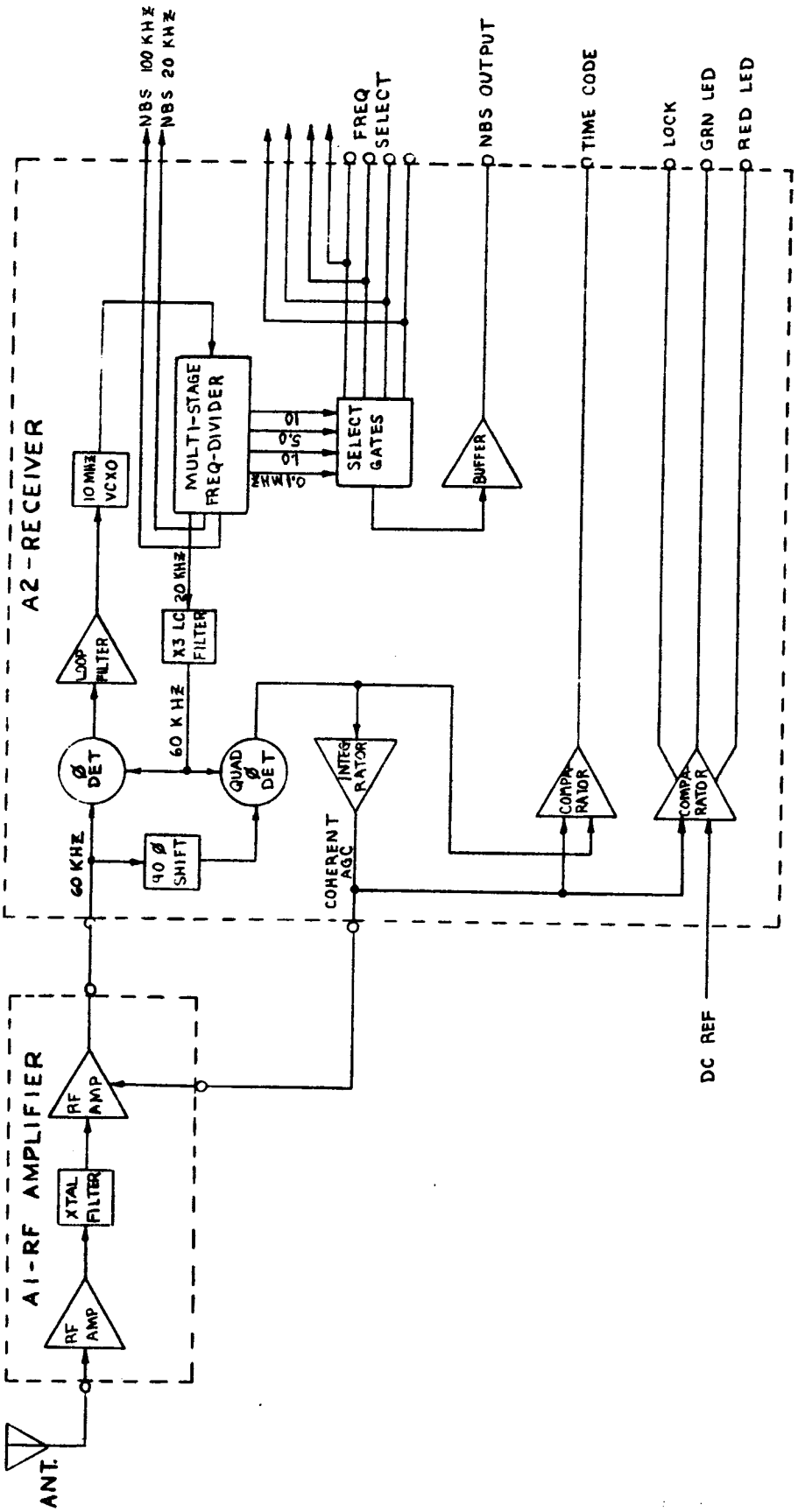


FIG. 2-2 RECEIVER BLOCK DIAGRAM

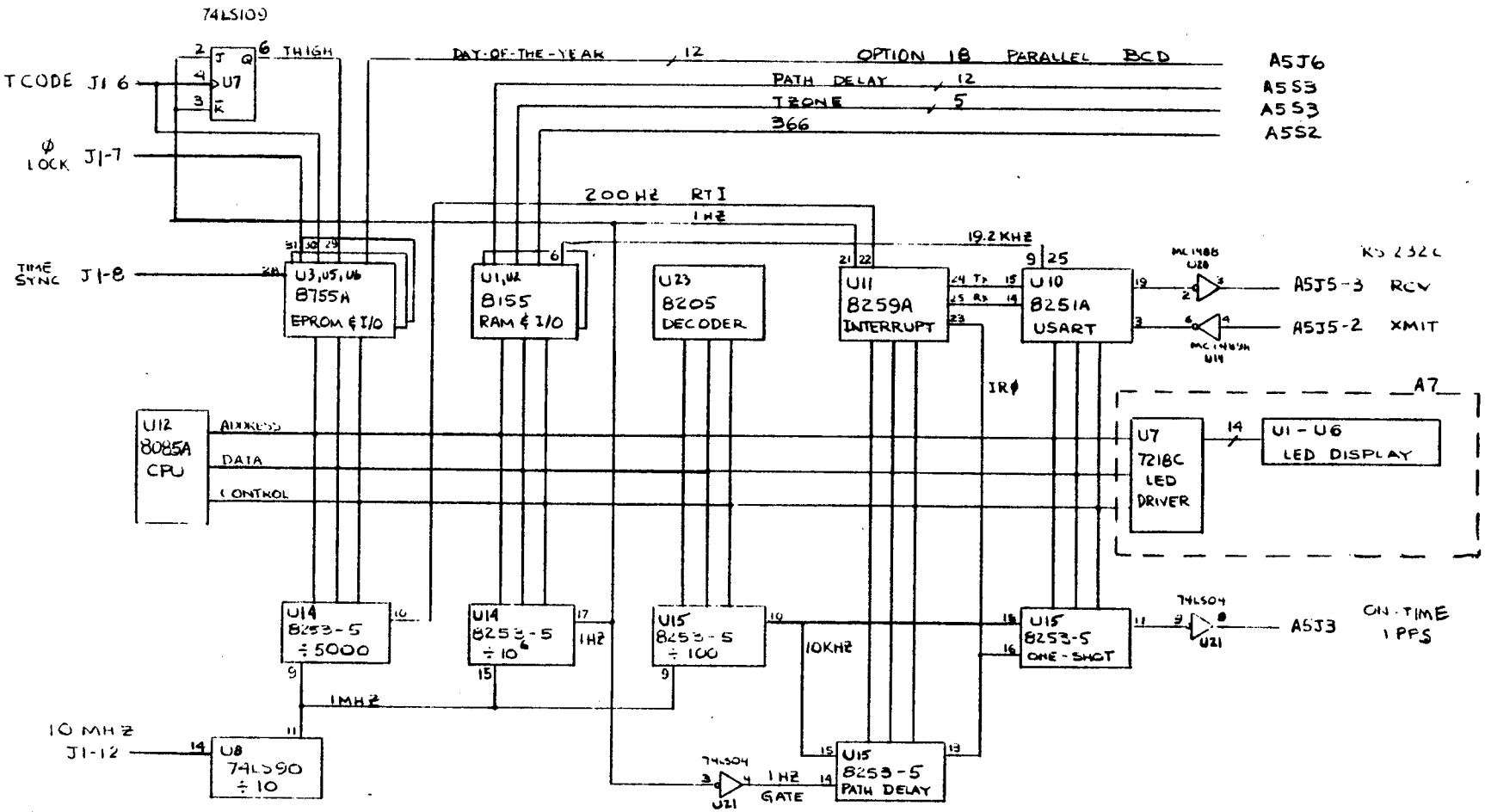


FIG. 2-3 MICROPROCESSOR BLOCK DIAGRAM

The output from the crystal filter is fed to amplifier U1, whose output is tuned with inductor L3 and capacitors C14, C15, and C23. Amplifier U1 is the stage that provides AGC for the receiver, with its gain control input port at pin 5. Trimmer resistor R19 provides AGC level adjustment.

The output of amplifier stage U1 is fed to the input of the second amplifier stage U2, the output of which goes to emitter follower Q3, providing the output signal to the A2 receiver assembly.

The supply voltage for the RF amplifier is +12 volts fed in at P2-1 and through R18, L2, and L1, to provide power for the amplifier stages. This power supply is also fed through switch S1 and resistor R2 to the input transformer where it goes out onto the antenna line to provide DC voltage to the preamplifier in the antenna. If switch S1 is moved to the P (Preamplifier) from the A (antenna) position the power supply is fed through R1 providing a smaller voltage drop so that both a series line preamplifier Model 8207, and the antenna may be powered from the receiver.

2.4 A2, RECEIVER ASSEMBLY, P/N 001200-1

When the signal from the RF amplifier assembly is fed into connector J5-3, it splits and goes in two directions. The first, through U1 and U2A, is the phase locked loop which provides synchronous detection of the carrier frequency and translates it to 10 MHz at the detector output. The second is through U3 and U2B to provide AGC voltage, time code detection, and phase lock/unlock indication.

Other functions of the A2 receiver assembly board include derivation of the rear panel 1-MHz NBS output signal from the 10-MHz phase locked oscillator and the power supplies. See Figure 2-5, sheets 1, 2 and 3.

2.4.1 Phase Locked Loop

The reference input to phase detector U1 pin 1 comes from the RF amplifier output (A1 assembly). The comparison frequency input to phase detector U1 pin 8 is derived from the phase locked oscillator, Q4 output. The output from U1 is a DC voltage which is a function of the phase difference of these 60-KHz signals. The output is amplified by U2A, the loop filter/amplifier. This amplified DC voltage is then fed through amplifiers Q2 and Q3 where it becomes the VCO control voltage which pulls the oscillator (Q4 and Y1) into phase lock relationship with the incoming carrier frequency from WWVB. This oscillator pulling is performed by the DC voltage which appears on the upper end of voltage variable capacitor CR2 controlling the "pulling" of crystal Y1. The oscillator output frequency is thus held at exactly 10 MHz by the DC voltage applied to the VCO control line. The

collector output from Q4 at BB is buffered by gate U5A and fed to a divider chain consisting of U8, U9, U10, and U16. A 1-MHz signal is selected and fed to the 1-MHz NBS output connector on the rear panel.

The 20-KHz output from U16 is fed to U18D and to the tripler stage Q9 where the output at 60 KHz is filtered and fed back at point AA into the comparison input of phase detector U1 pin 8. Thus, the phase locked loop translates the incoming 60-KHz carrier frequency from WWVB to 10 MHz at the crystal oscillator output, and divides it down to 60 KHz for comparison in the phase detector.

2.4.2 AGC Loop

The input from the RF amplifier also goes to pin 1 of phase detector U3 after being shifted in phase by 90° by C14, C15, and L1. Thus, U3 becomes a quadrature phase detector whose output at pin 6 goes high only when the inputs at pin 1 and pin 8 are in quadrature with each other at 60 KHz. The output level from this phase detector is proportional to the level of the incoming carrier, and thus provides the basis for time code amplitude detection, and for AGC voltage generation.

The phase detector output is amplified by U2B, whose time constant is approximately 15 milliseconds. The output of U2B is split and is fed in two directions: first through R39 to voltage comparator U4A where small amplitude variations in the signal are detected and provide the time code output.

The output of U2B also is fed through R89 to amplifier U2C which has an integrating time constant of approximately 25 seconds. The slowly varying output of U2C is used as the AGC voltage and is fed back to the RF amplifier to control the gain of the input stage.

Because the AGC voltage is derived from the output of a quadrature detector, it is present only after phase lock is achieved, and thus becomes the basis for a synchronous AGC. The gain of the amplifier in the front end of the receiver is running wide open until phase lock occurs. After phase lock is acquired the input amplifier gain is reduced to a level just sufficient to provide a reference for the phase locked loop and other stages in the A2 receiver assembly. Thus, no stages in the A2 receiver assembly are allowed to saturate or be overdriven in strong signal conditions.

Test point 3 is located at the reference voltage against which AGC amplifier U2C operates. Thus, the voltage measured from TP3 to TP6 is proportional to the input signal level, and can be used as a synchronous detector, or "lock-in voltmeter", as an indication of signal strength. If the antenna is adjusted and aimed to maximize this AGC voltage, optimum receiver operation is obtained.

The AGC voltage is also sent to voltage comparators U4B, U4C, and U4D as a means of indicating phase lock. When the AGC voltage measured between test points 3 and 6 rises to approximately 1.0 volt DC, the output of comparator U4B goes high turning off the red unlock panel indicator on the front panel. When lock is acquired and the green light goes on, the output of U4D goes high showing that phase lock has been acquired.

2.4.3 Phase Detector Balance Adjustment

The output of phase detector U1 for the phase locked loop control is balanced by adjustment of trimmer potentiometer R5. (See alignment procedure for A2 receiver assembly.) The output of the quadrature phase detector U3 is balanced by adjustment of trimmer potentiometer R30. (See alignment procedure for A2 receiver assembly.)

2.4.4 Power Supplies

Three-terminal regulators U21, U22 and U23 provide output voltages of +5.0 volts, +12.0 volts, and -12.0 volts. Because U21 which provides the +5.0 volts is the most heavily loaded of the voltage regulators, it is heat sunk to the chassis at the rear left corner of the circuit board. Regulators U22 and U23 are loaded more lightly and do not require heat sinking.

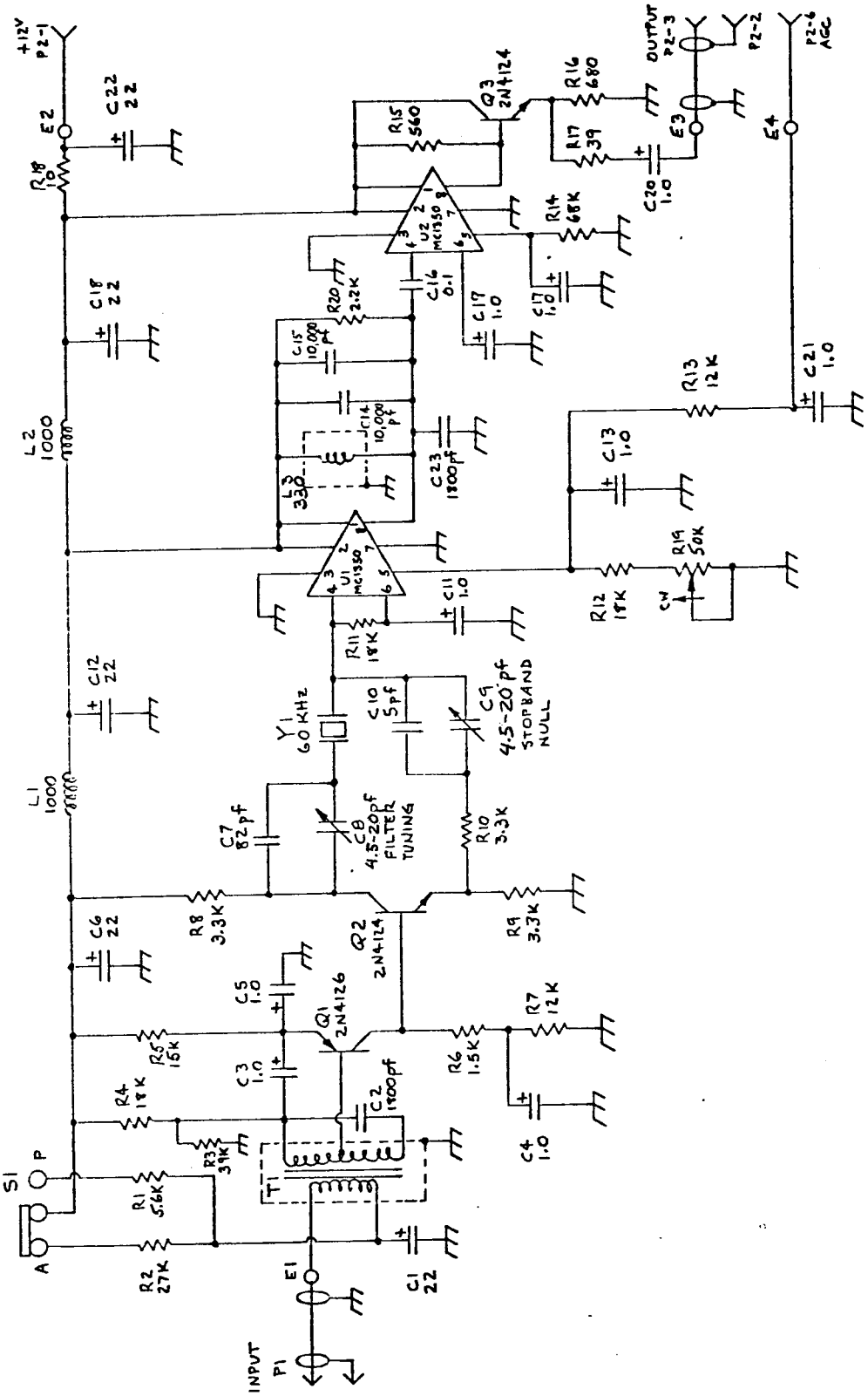


FIG. 2-4 SCHEMATIC - A1 RF AMPLIFIER

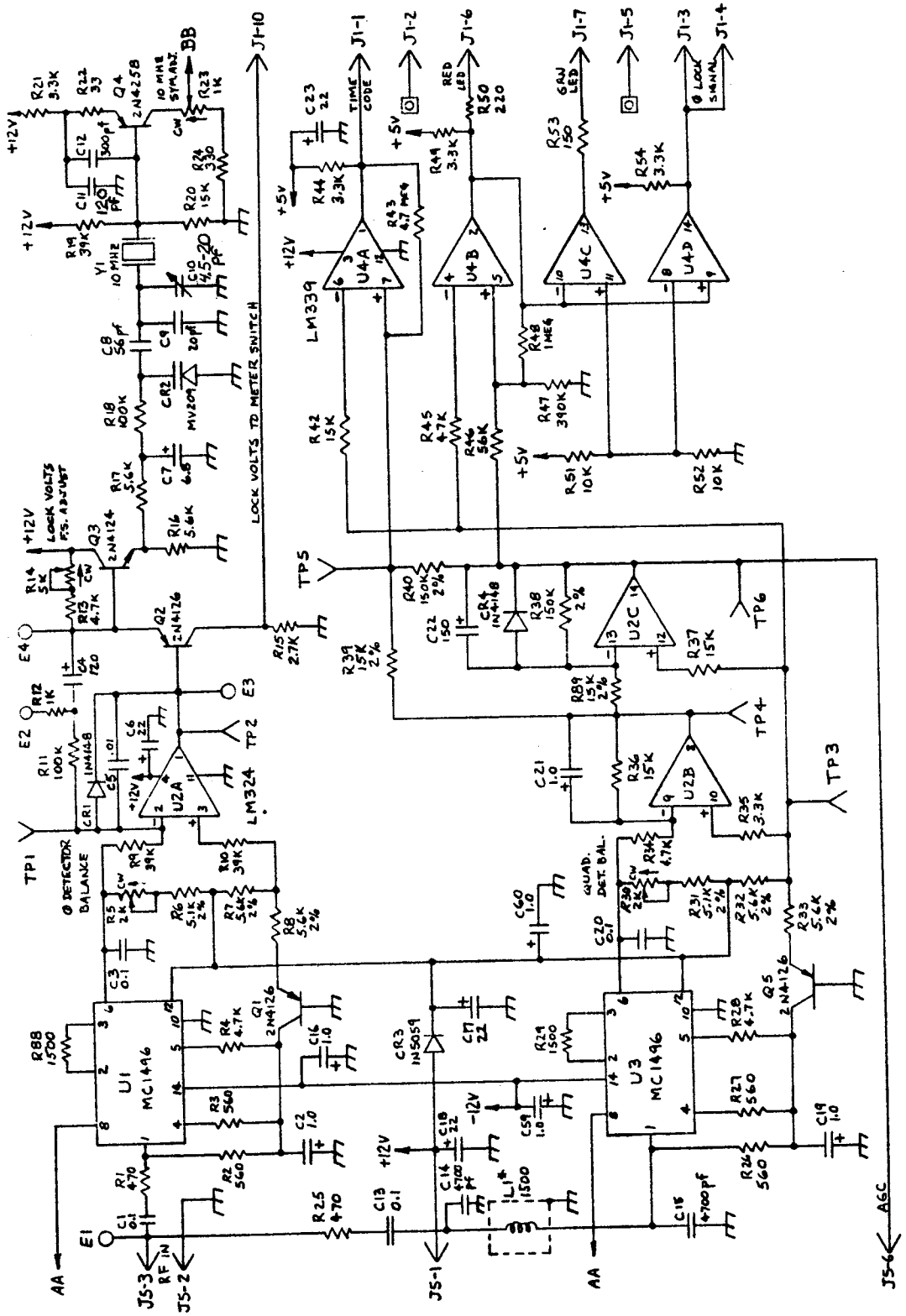


FIG. 2-5 SCHEMATIC - A2 RECEIVER - SHEET 1

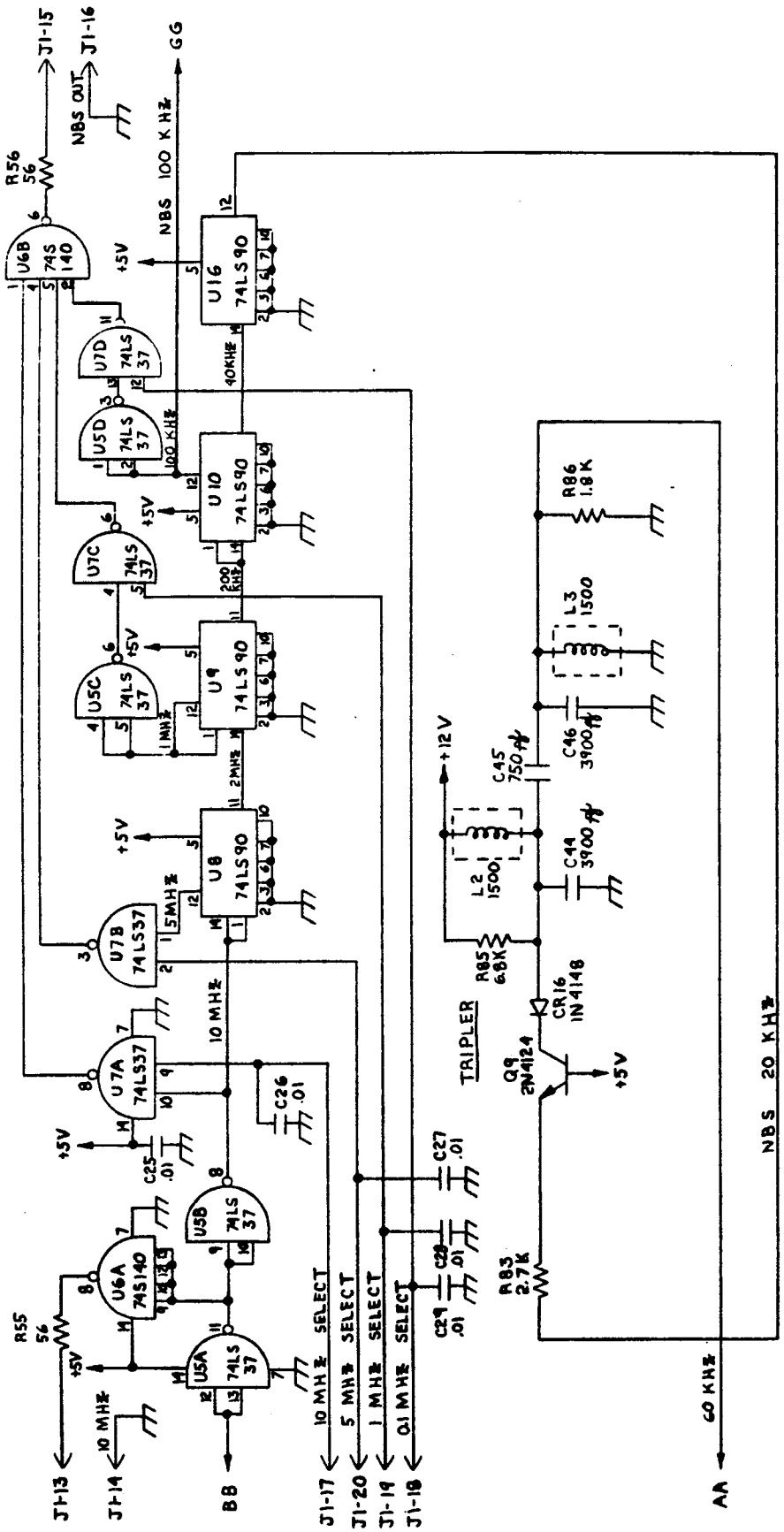


FIG. 2-5 SCHEMATIC - A2 RECEIVER - SHEET 2

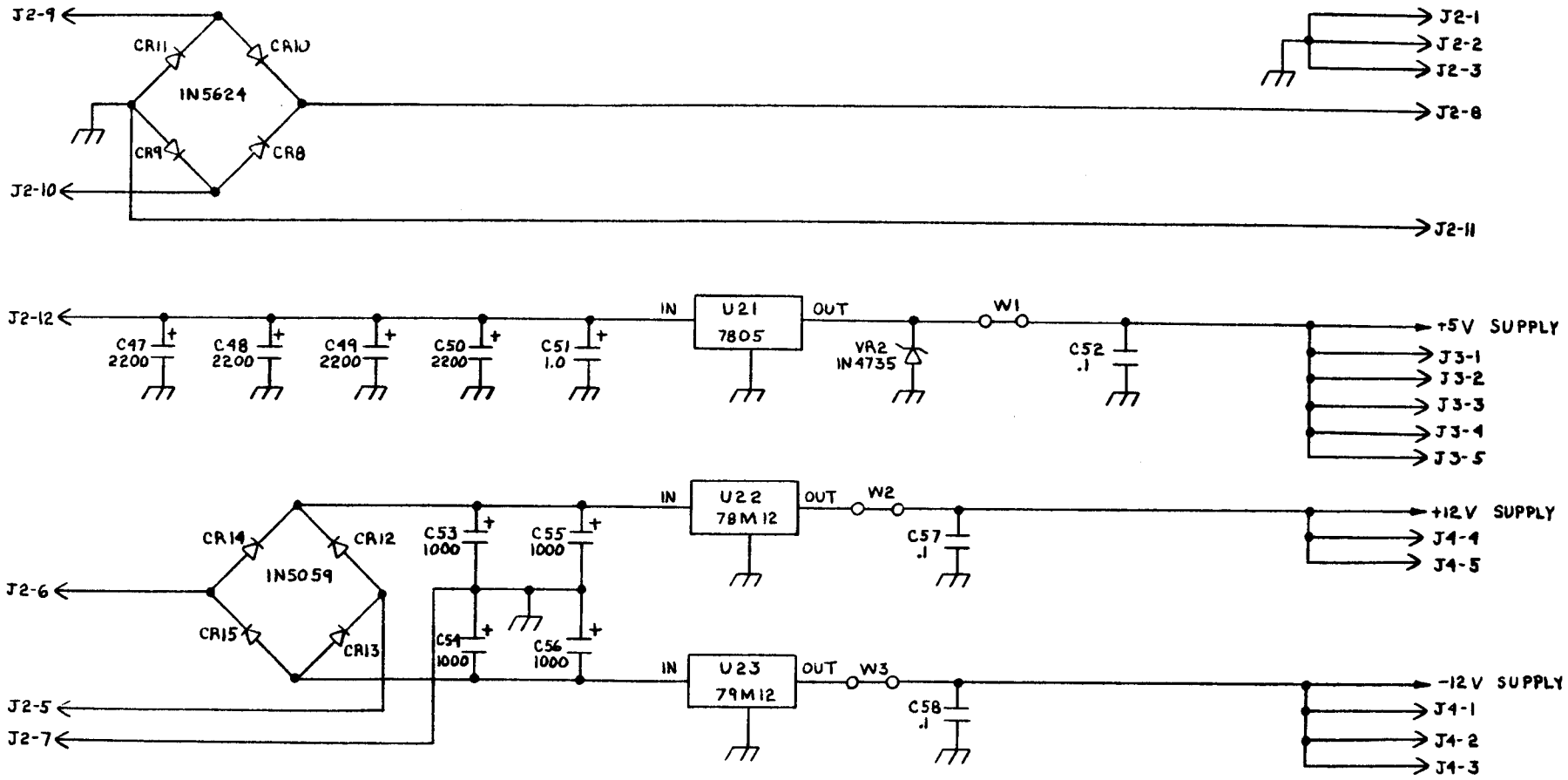


FIG. 2-5 SCHEMATIC - A2 RECEIVER - SHEET 3

2.5 A3, MICROPROCESSOR ASSEMBLY, P/N 014800

The 10-MHz NBS phase locked signal is fed into U8 and divided by 10 to 1 MHz. (See Figure 2-3 Processor Block Diagram). This signal is divided by 5000 by U14A to provide a 200-Hz real-time interrupt, and it is divided by 1,000,000 by U14B and U14C to provide the 1-Hz on-time reference. It is divided by 100 by U15A to provide a 10-KHz signal which is fed as a clock input to path delay timer U15B. The path delay timer is gated on by the 1-Hz reference. An output pulse will occur after a delay proportional to the setting of the path delay thumbwheel switch on the rear panel. The signal is fed into U15C, which is a programmable one-shot. The output is a 100-millisecond pulse whose leading edge is "on-time".

The time code, TCODE, signal is fed to input U5-30 on the 8755A and to U8-4, the clock input to a 74LS109 J-K flip-flop. The TCODE is sampled at a 5-millisecond rate by the microprocessor. False noise pulses are discarded. The pulse widths are measured and decoded and the 1-Hz reference signal is phase locked to the leading edge of the time code.

The phase lock algorithm has two modes, fast sync and fine sync. In the fast sync mode, the 1-Hz reference is adjusted in 0.1-second steps until phase lock is achieved. The adjustment steps are progressively reduced to 1 millisecond. After the clock is set the steps are reduced to 0.1 millisecond. The time between adjustments is made progressively longer and will extend beyond 24 hours. Each time an adjustment is made the time and direction of the adjustment is logged in the Phase Adjust Table (See Section 1).

A serial RS-232 interface is provided by U10, 8251A USART and U26 and U19 level converters.

The program resides in U6, U5 and U3, 8755A EPROM & I/O. Variable data is stored in 512 bytes of RAM in U1 and U2 8155 RAM & I/O.

The processor runs under interrupt, with priorities controlled by U11 8259A Programmable Interrupt Control Chip.

The interrupt levels are:

- IR0 - On-time pulse
- IR1 - Irig Frame Element (Option 23)
- IR2 - Remote Output USART Xmit (Option 19)
- IR3 - 1 Hz reference
- IR4 - 200 Hz RTI
- IR6 - USART Xmit
- IR7 - USART Rcv

Chip selects are decoded by U23 and U30 8205 1-8 Decoder. The chip selects are:

CS0 - U5-1	8755A	EPROM & I/O
CS1 - U23-14	8155	RAM 7 I/O
CS2 - U14-21	8253-5	TIMER
CS3 - U15-21	8253-5	TIMER
CS4 - U3-1	8755A	EPROM & I/O
CS5 - U22-5	74LS02	LED DISPLAY
CS6 - U11-1	8259A	PROGRAMMABLE INTERRUPT CONTROLLER
CS7 - U10-1	8251A	USART
S0 - U4-6	8255A	PROGRAMMABLE PERIPHERAL INTERFACE (Option 18)
S1 - U9-11	8251A	USART (Option 19)
S2 - U17-21	8253-5	TIMER (Option 23)
S3 - U16-21	8253-5	TIMER (Option 23)
S4 - U2-8	8155	RAM & I/O
S5 - U6-1	8755A	EPROM & I/O

The central processing unit U12 is an 8085A with a 6.14-MHz crystal. Power-on reset is provided on pin 36 by a brown-out reset network. Signals RD, WR and RDY are tied to +5 volts through Resistors R3, R11 and R2.

The 555 Timer, U24 sheet 6, is an Astable oscillator that generates a negative 20 millisecond reset pulse every 1.9 seconds. The retriggerable monostable multivibrator, U21B, is triggered once per second by a pulse that is generated by the program. The output of the one-shot inhibits the reset pulse from the Timer (Gate U22). On power up or if the normal program is stopped, the one-shot times out and a reset pulse is applied to the microprocessor.

The detail schematics for the Microprocessor boards are shown in Figure 2-6, sheets 1 through 6.

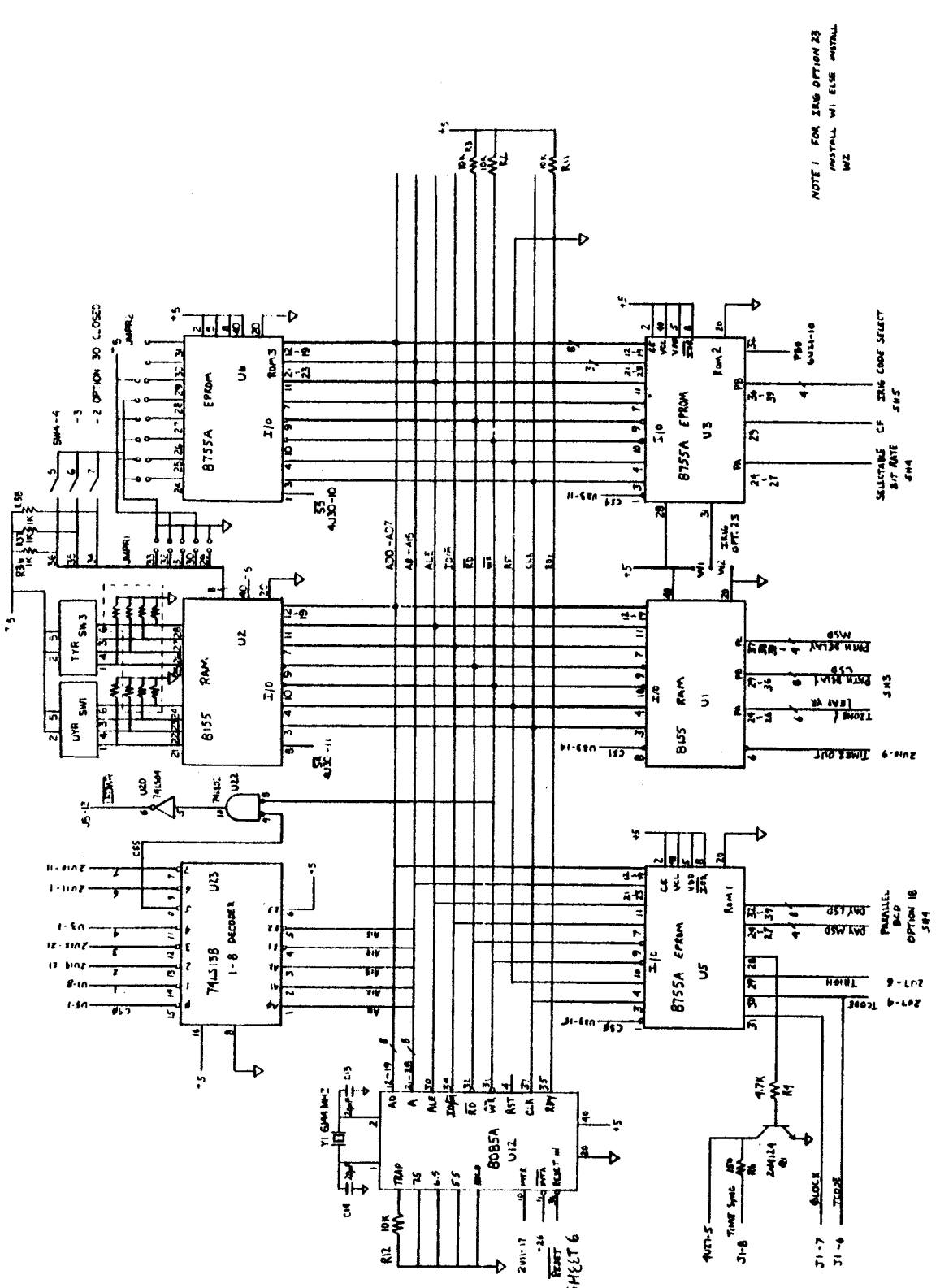


FIG. 2-6 A3 MICROPROCESSOR - SCHEMATIC - SHEET 1

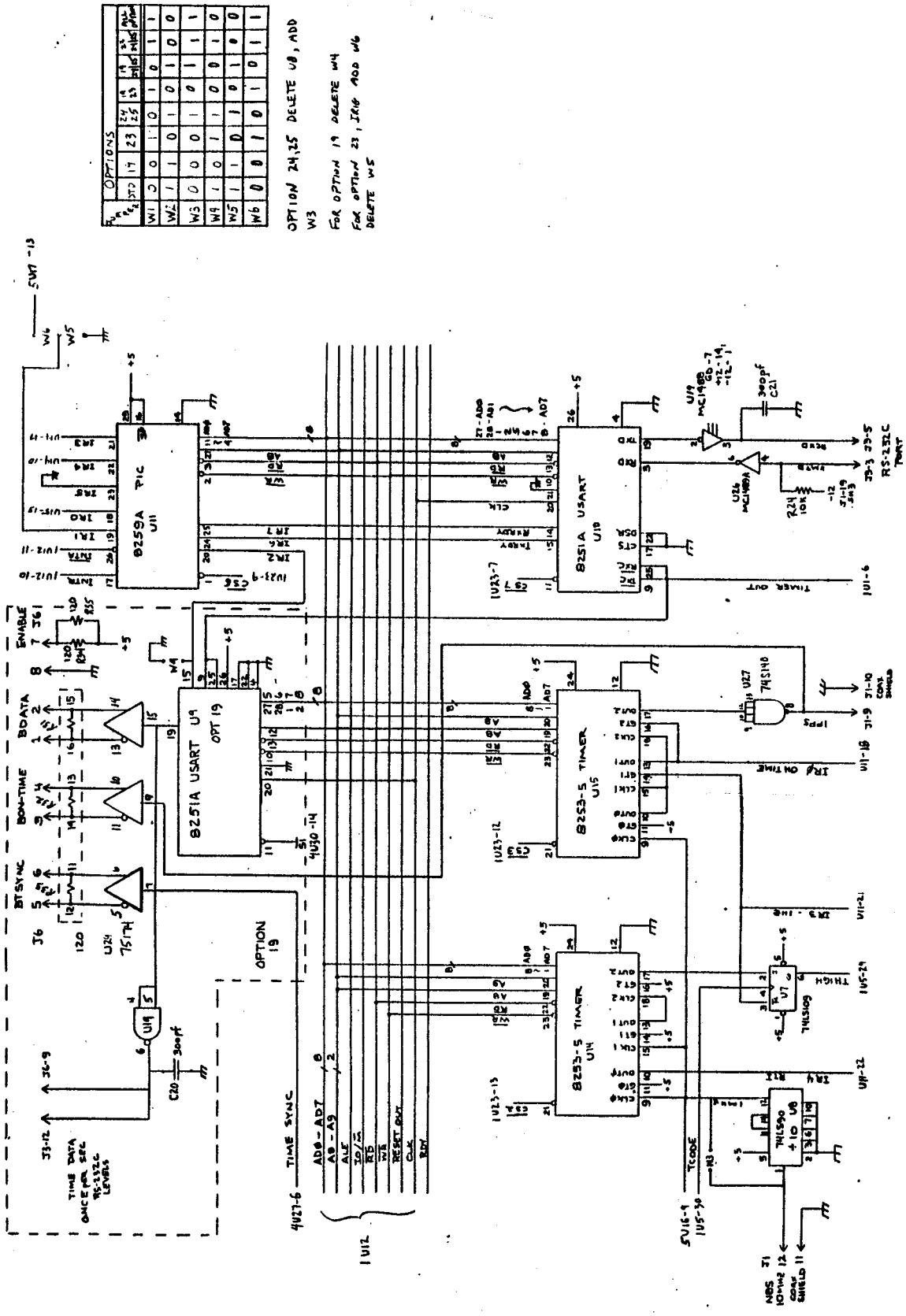


FIG. 2-6 A3 MICROPROCESSOR - SCHEMATIC - SHEET 2

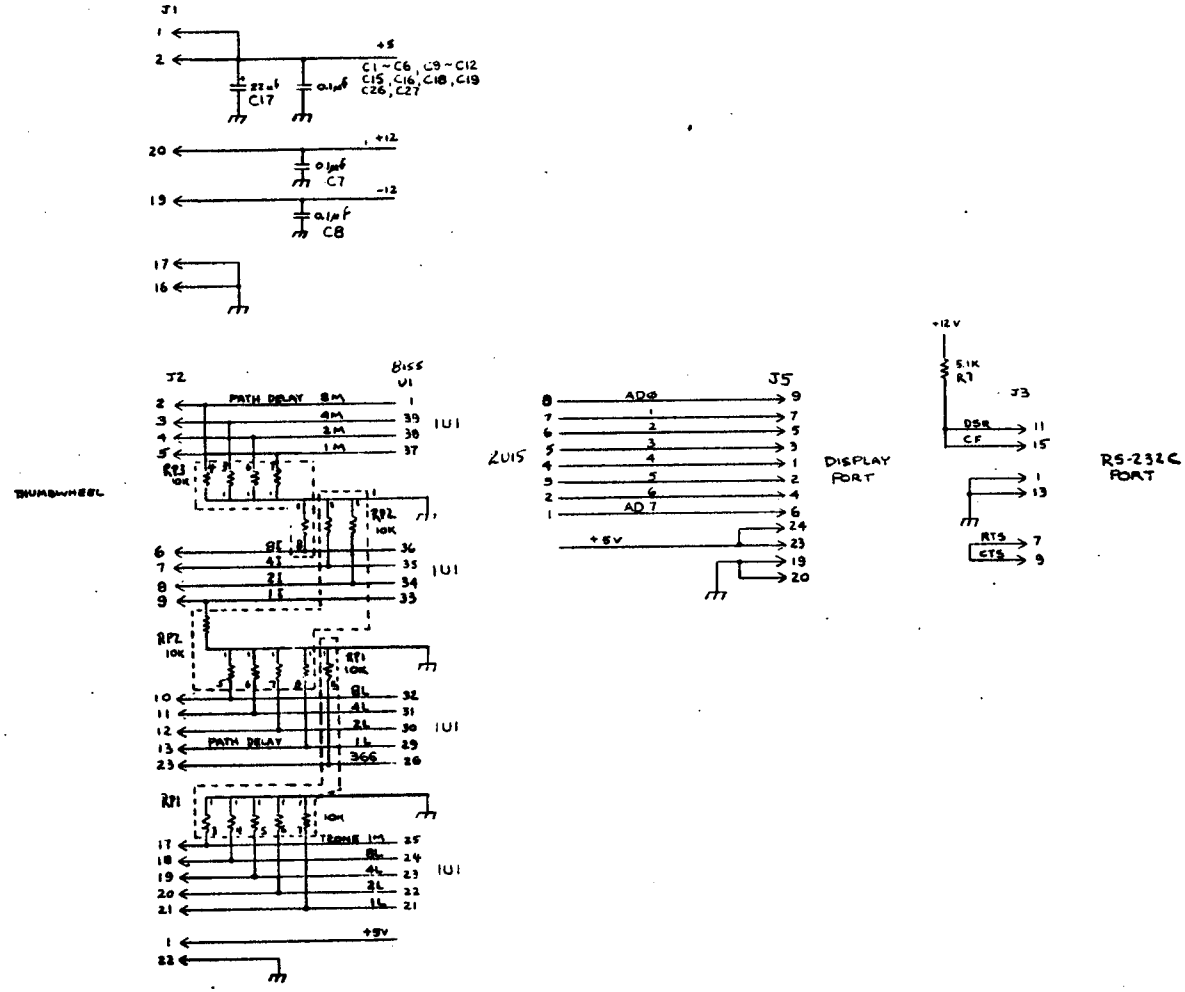


FIG. 2-6 A3 MICROPROCESSOR - SCHEMATIC - SHEET 3

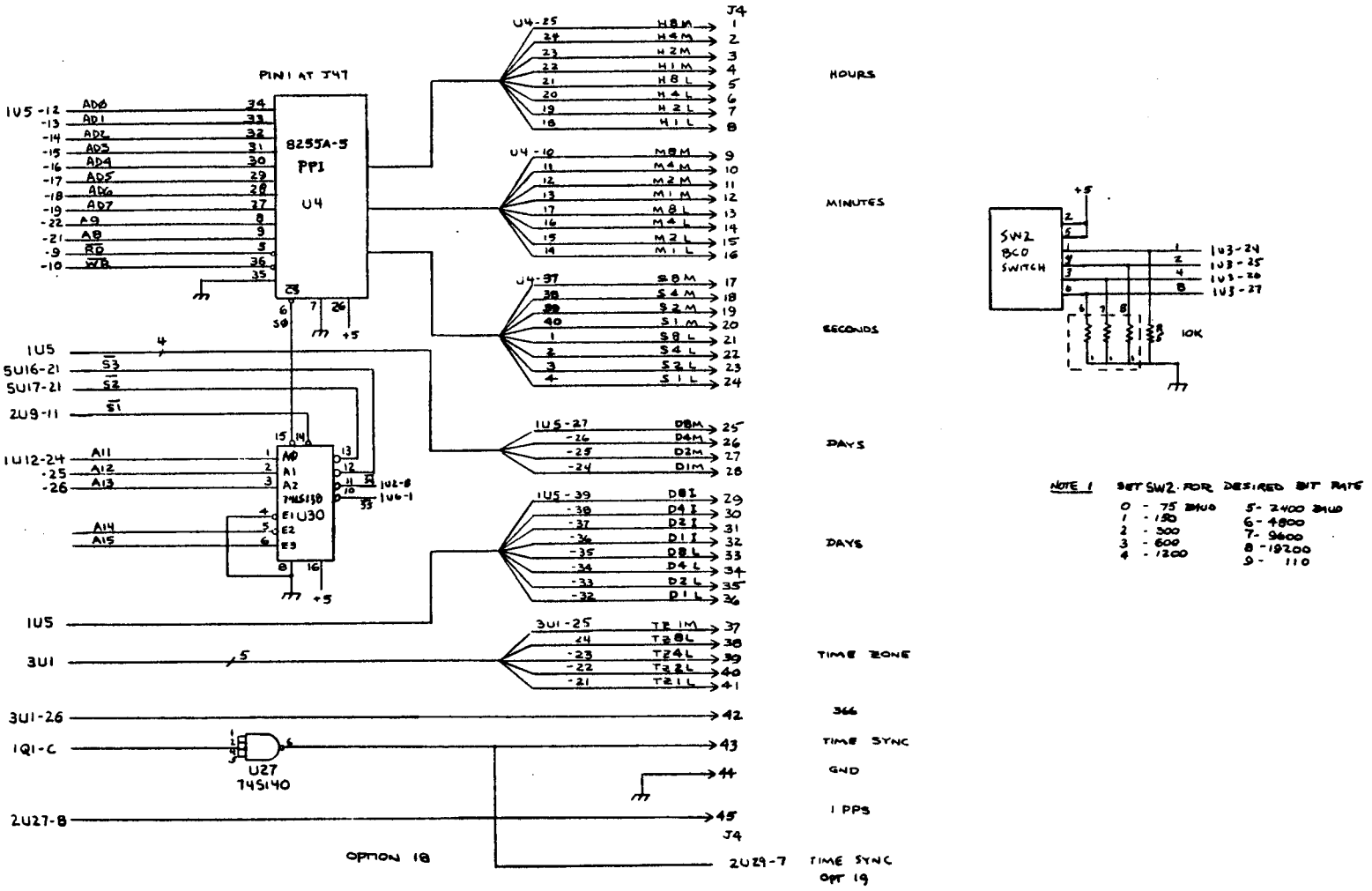


FIG. 2-6 A3 MICROPROCESSOR - SCHEMATIC - SHEET 4

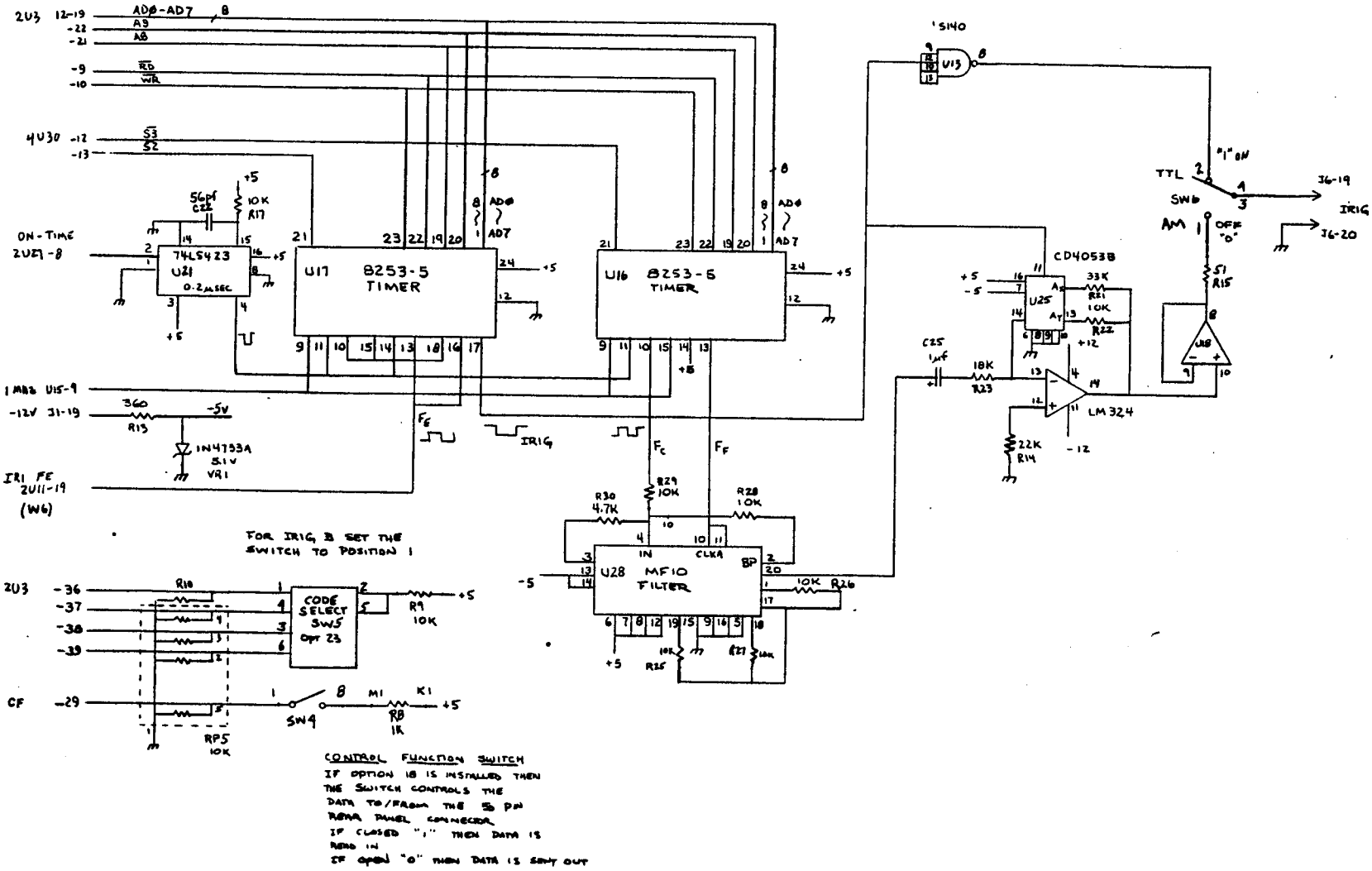


FIG. 2-6 A3 MICROPROCESSOR - SCHEMATIC - SHEET 5

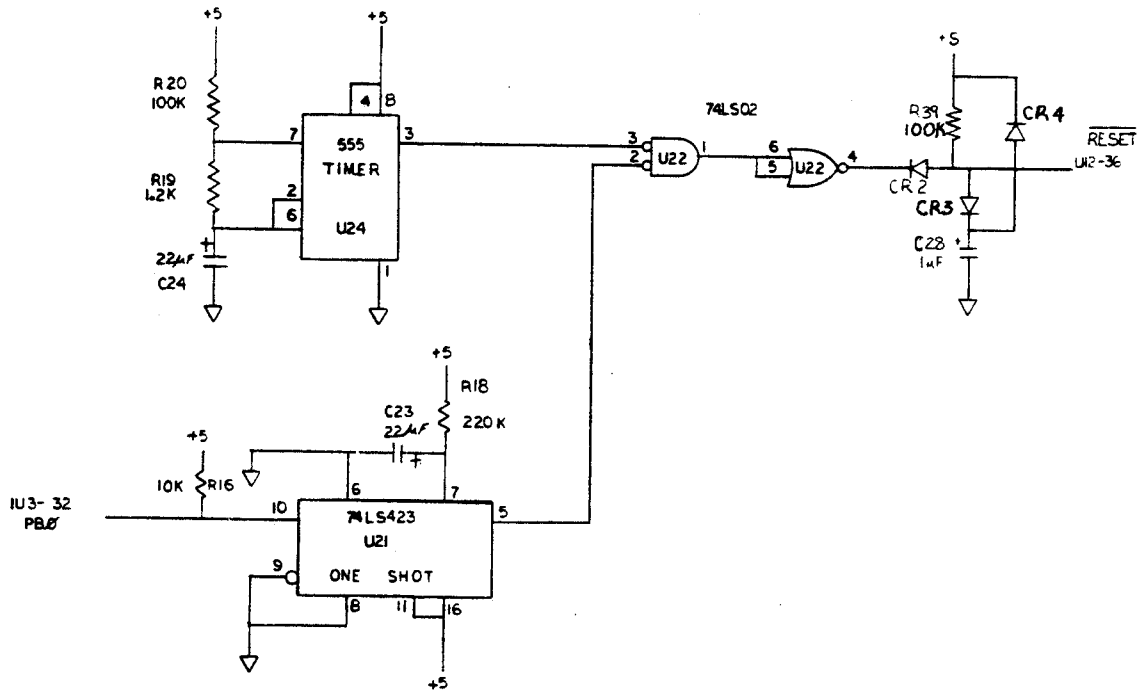


FIG. 2-6 A3 MICROPROCESSOR - SCHEMATIC - SHEET 6

2.6 A4, DISPLAY ASSEMBLY, P/N 014100

The display assembly is mounted on the rear of the front panel. It consists of U7-ICM7218C LED Driver and six seven-segment LED digits that provide a 24-hour clock display (See Figure 2-7.)

2.7 POWER TRANSFORMER

The AC power schematic, Figure 2-8, shows the AC input for the +5 VDC, +12 VDC and -12 VDC power supplies. The AC input A6 is filtered by C1 and C2, then fed through fuse F1 and 115/230V switch S1 to transformer T1.

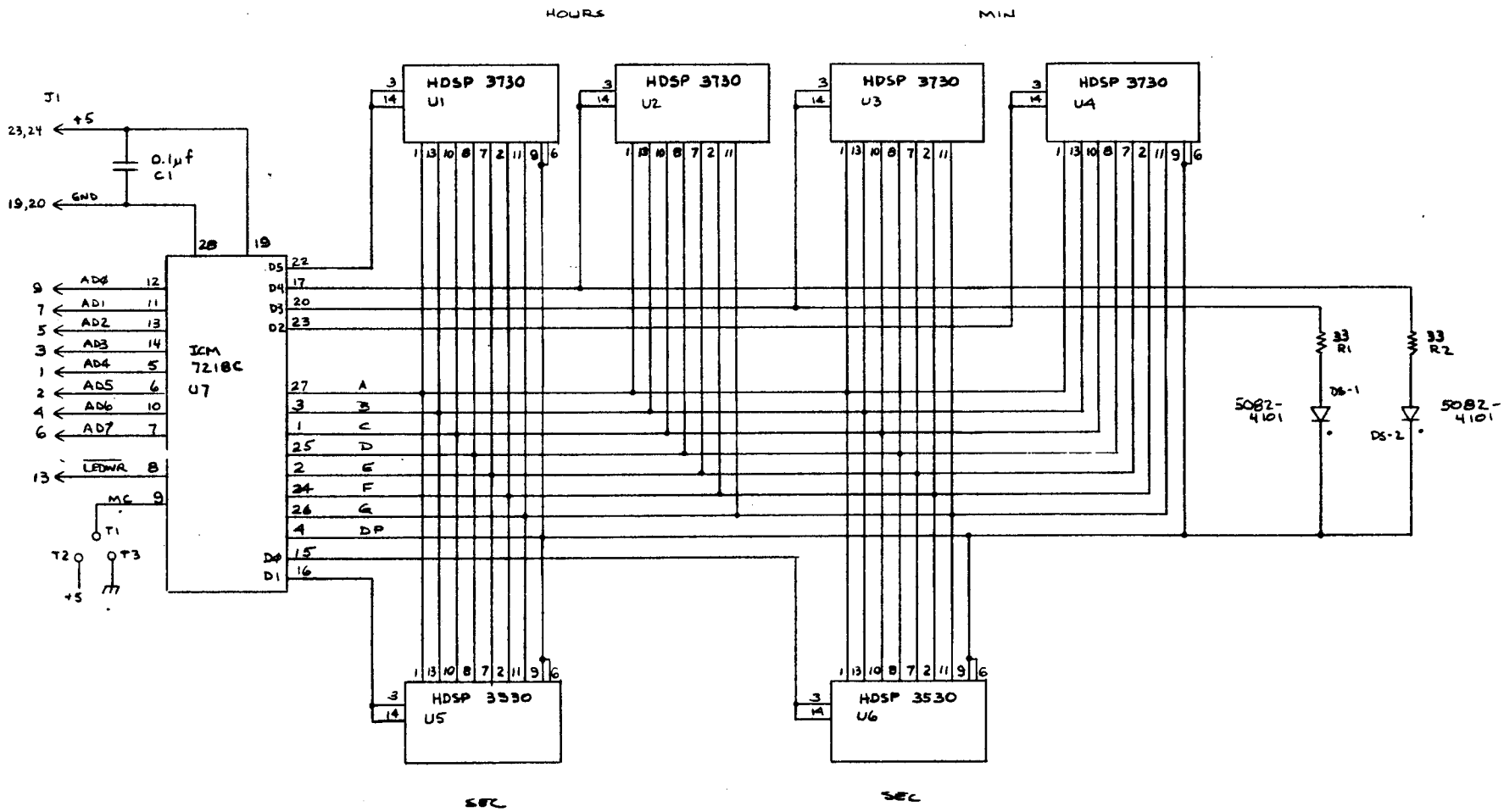


FIG. 2-7 A4 SCHEMATIC

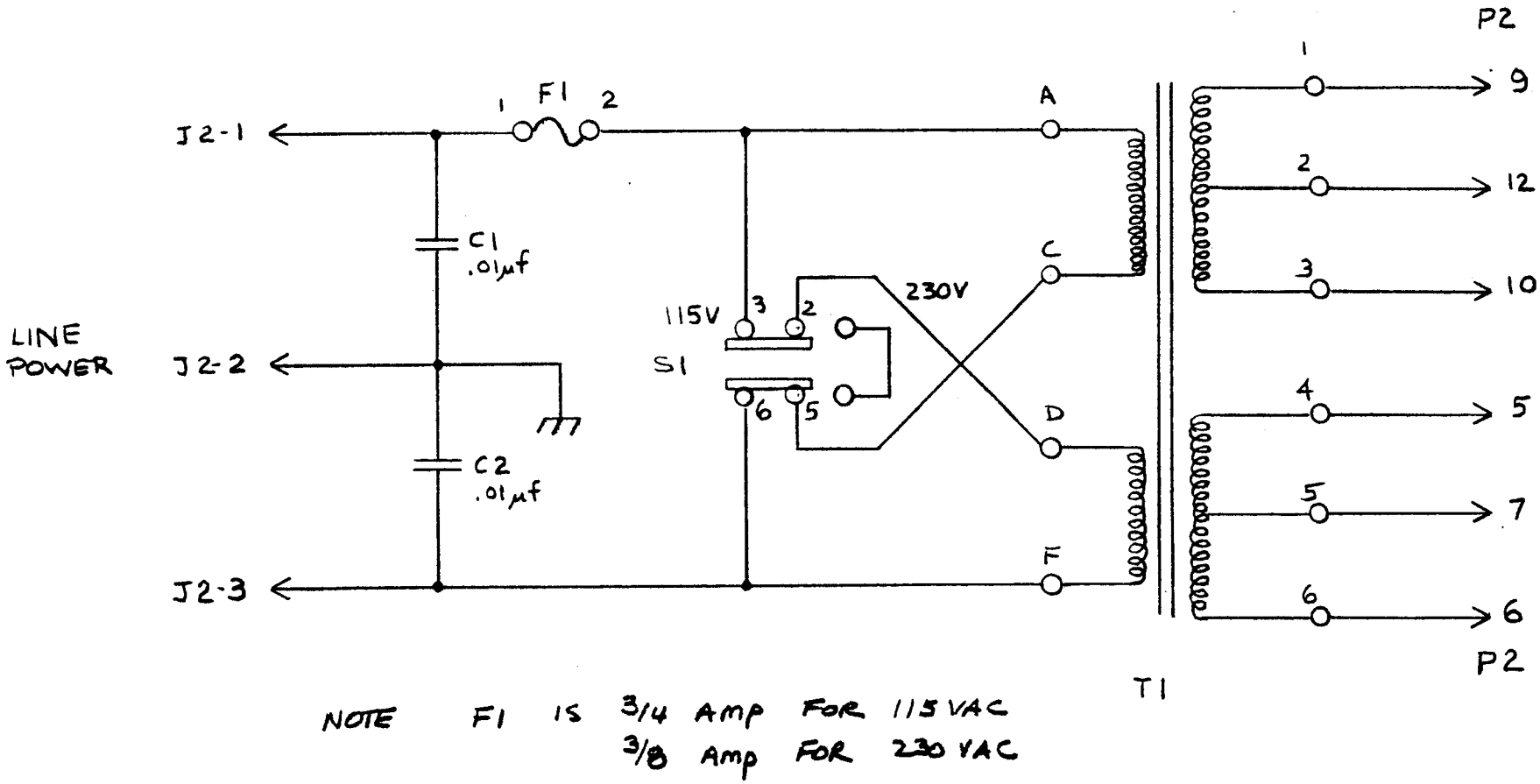


FIG. 2-8 AC POWER DIAGRAM

SECTION 3

8170

SERVICE INFORMATION

3.1 CALIBRATION OF THE MODEL 8170

The Model 8170 is "connected" to the National Bureau of Standards time standard via radio signals. The instrument automatically decodes the time transmitted by WWVB. Varification of proper operation can be made by tuning a HF receiver to WWVB and comparing the voice time announcements against the Model 8170. Alternatively, the audio portion of WWVB may be heard by calling 303-499-7111. Accuracy of the time signal received over the telephone is 30 milliseconds anywhere in the contiguous 48 states.

For precise calibration, a portable clock calibrated at NBS is required. Connect one trace of an oscilloscope to the On-time pulse output of the 8170 and the other trace to the On-time pulse from the portable clock. Set the path delay thumbwheel switch on the rear panel to 00.0. Synchronize the scope with the portable clock on-time pulse, adjust the path delay switch until the two pulses are coincident. The setting of the switch is the sum of the path delay and receiver delay in milliseconds.

In some applications it may be desirable to calibrate a group of clocks against one reference clock. This provides accurate relative time between the ensemble of clocks. The calibration procedure is the same as with the portable clock example, except an 8170 reference clock is used in place of the portable clock.

3.2 ALIGNMENT PROCEDURES

Figure 3-1 Assembly drawing shows the location of the major assemblies.

3.2.1 RF Amplifier Assembly (A1 Board, Figure 3-2)

1. Disconnect the AGC wire (violet) from Connector A1P2 pin 6, but leave the remaining wires in place and the connector mated.

2. Connect an oscilloscope probe to A2E1. Set the scope for AC coupling. The ground lead is connected to the chassis.

3. Connect a signal generator to the antenna input of the receiver. Set the generator to provide a 1.0 uV signal at exactly 60,000 Hz, unmodulated.

4. Apply power to the receiver and adjust the signal generator level as necessary to provide a 1 volt p-p output signal on the oscilloscope.

5. Adjust the slug in transformer A1T1 for a peak on the oscilloscope, while reducing the signal generator level to maintain the 1V p-p output.

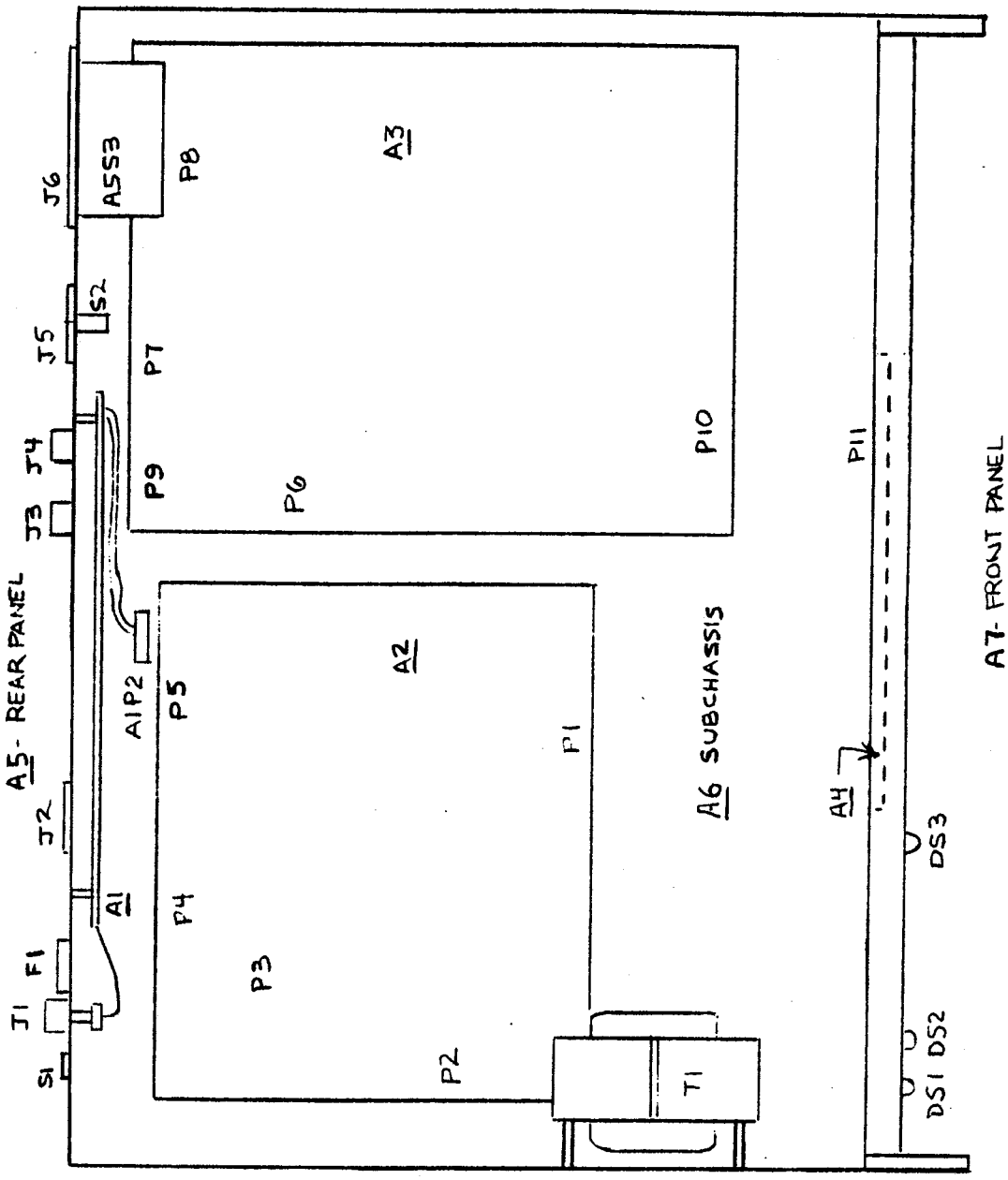


FIG. 3-1 ASSEMBLY DRAWING - MAINFRAME

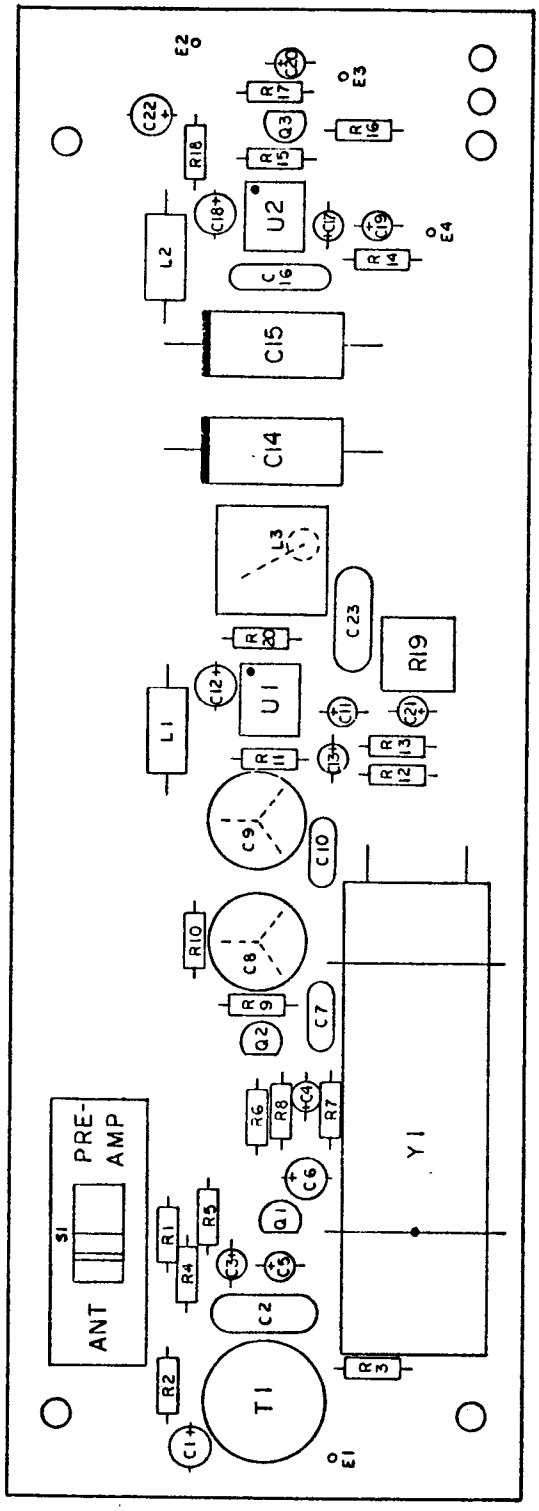


FIG. 3-2 A1 RF AMPLIFIER ASSEMBLY

6. Adjust capacitor A1C8 for maximum output on the scope.

7. Readjust the signal generator frequency to 100,000 Hz and increase the output for a reading of 1V p-p on the oscilloscope (Do not exceed 0.1 volt at the antenna input).

8. Adjust capacitor A1C9 for minimum output on the oscilloscope, while increasing the signal generator level to maintain 1V p-p output (Do not exceed 0.1 volt at the antenna input).

9. Readjust the signal generator output frequency to 60.000 KHz at a 1 mV level.

10. Synchronize the oscilloscope, and observe the output waveform and level. The output should be a square wave with a 40-60% duty cycle and 3V p-p $\pm$ 20% amplitude.

11. Set the signal generator output level at 5 uV. The oscilloscope amplitude should equal or exceed 1.5V p-p (the output will be a sine wave until the clipping point is reached at approximately 3V p-p).

12. The AGC Alignment is performed as described in step 17 of the Receiver Assembly (A2 board) procedure described below.

13. Disconnect the oscilloscope and signal generator.

3.2.2 Receiver Assembly (A2 Board, Figure 3-3)

1. Connect a clip lead from A2E2 to A2E3. Connect the negative lead of a DVM to test point A2TP3 and the positive lead to test point A2TP4. Set the DVM for a full scale range of $\pm$ 2V. There should be no connection to the antenna input at this time.

2. Apply power to the receiver. The DVM should read zero $\pm$ 5 mV. If the voltage error is greater than $\pm$5 mV, adjust potentiometer A2R30. Some variation will be noted, but it should be less than $\pm$ 5 mV.

3. Move the positive DVM lead from test point A2TP4 to A2TP6. The reading should be less than 500 mV. Glyptol A2R30 if it has been adjusted.

4. Move the positive DVM lead to test point A2TP2 and the negative DVM lead to A2TP1.

5. The DVM reading should be zero $\pm$5 mV as observed in step 2 above. If the voltage error is greater than $\pm$5 mV, adjust potentiometer A2R5.

6. Remove both DVM leads from the test points and turn off the receiver.

7. Move the clip lead from A2E3 to A2E4 (A2E2 jumpered to A2E4). Connect the positive lead of a 0-1 mA meter to A2J1-10.

8. Apply power to the receiver. The meter should read 0.8 mA. If it does not, adjust potentiometer A2R14. Glyptol A2R14 if it has been adjusted.

9. Connect a frequency counter to the 10 MHz NBS output on A2J1-13. The counter should read 9,999.900 KHz (9.999900 MHz). If necessary, adjust capacitor A2C10 to obtain this reading. Disconnect the frequency counter and the clip lead from A2E2 to A2E4.

10. Connect the 10 MHz NBS output on A2J1-13 to a spectrum analyzer or selective voltmeter through a suitable attenuater.

11. Adjust potentiometer A2R23 for a minimum 2nd harmonic (20 MHz) on the spectrum analyzer. It should be adjustable to at least -20 dB relative to the 10 MHz output. Glyptol A2R23.

12. Connect a signal generator to the receiver antenna input, set a 1 mV output at 60.000 KHz unmodulated. The receiver should lock to this signal as indicated by the green lock lamp being lit. Measure the VCO lock voltage by connecting the positive lead of a 0-1 mA meter to A2J1-10. If necessary, adjust capacitor A2C10 very slowly until the lock voltage is exactly at center scale.

13. Disconnect the signal generator from the receiver antenna input and note the lock voltage meter reading on the milliammeter (disregard any sudden small jump at the moment of disconnection). If a downward drift is observed, adjust A2R5 clockwise by very small amounts until the drift is stopped (small jumps may occur as the potentiometer is adjusted, disregard these and note only the slow drift). Conversely, if an upward drift is observed, adjust potentiometer A2R5 CCW by very small amounts until the drift is stopped. This is a very fine adjustment, and is completed when no perceptible drift is evident after one minute of observation. Glyptol the potentiometer if it has been adjusted.

14. Connect the signal generator to the receiver antenna input and set it for a 1.0 microvolt level at 60.000 KHz, unmodulated.

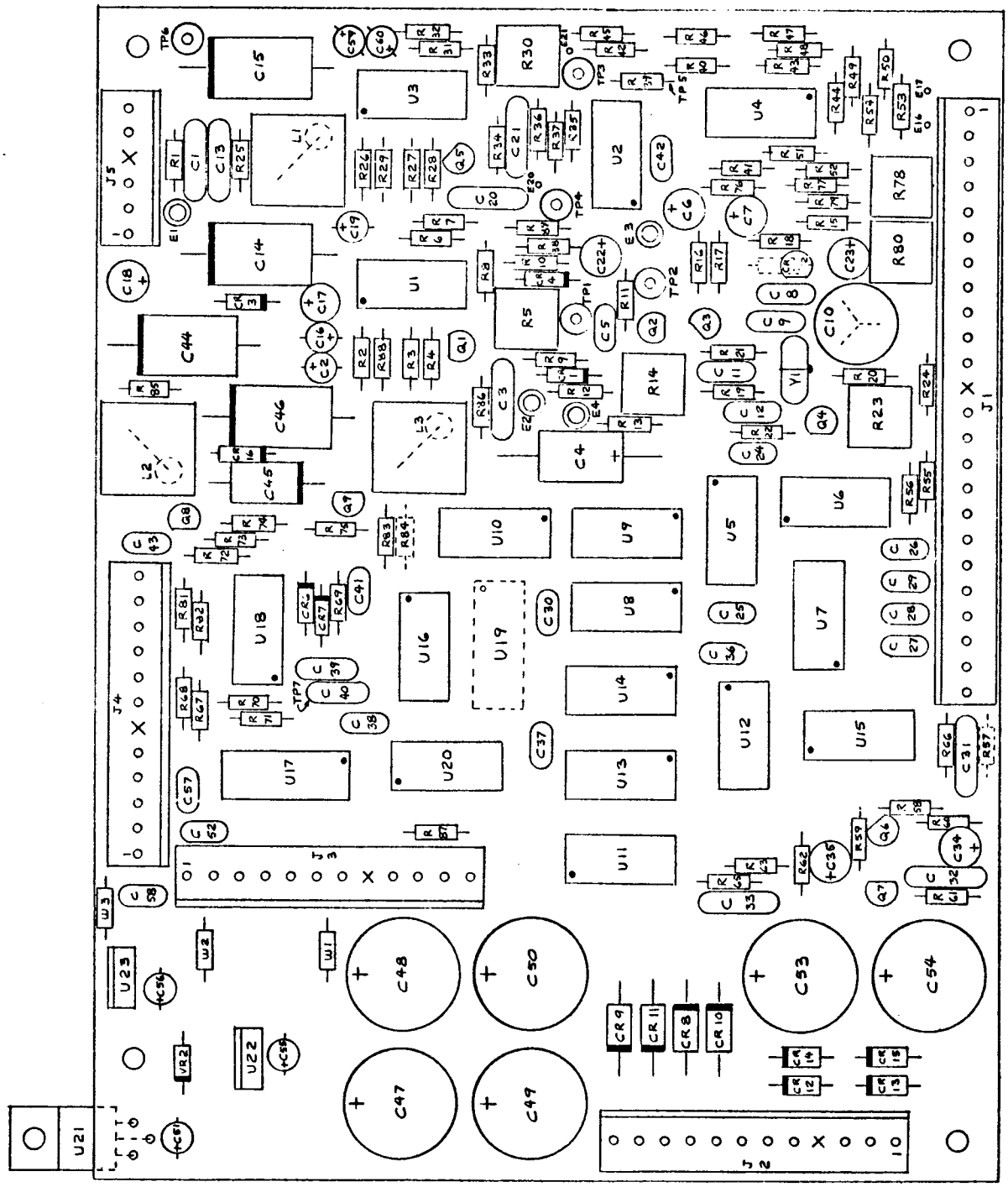


FIG. 3-3 A2 RECEIVER ASSEMBLY

15. Connect the negative lead of a DVM to test point A2TP3. Select a scale in the +5 to +20 VDC range and connect the positive lead to test point A2TP6. The reading should increase to greater than 2.38V after the receiver has locked (green light on). Lock-up may take several minutes at the 1.0 uV input, and the voltage at test point A2TP6 may continue to rise after the green lock light has lit.

16. After the voltage at the above test point has exceeded +2.38V, decrease the signal generator output level by small amounts (less than 1 dB) until the voltage has decreased to +2.38V. When approaching the correct voltage it will be necessary to wait one minute or more between signal generator level changes, as the voltage read on the DVM is delayed by a 90-second time constant from the initiation of change. A +2.38V reading at test point A2TP6 is normally reached with an antenna input level between 0.25 and 1.0 uV.

17. Without changing the signal generator level from that obtained in step 16 above, reconnect the violet AGC wire to pin 6 of connector A1P2 (see step 1, RF Amplifier Assembly). The DVM reading will slowly decrease and stabilize at +1.38 volts. If the DVM stabilizes at a different reading, adjust the AGC control potentiometer, A1R19, on the RF Amplifier Assembly (A1) in very small amounts until the meter reading stabilizes at 1.38 volts. A wait of one minute or more between pot settings may be necessary due to the long time constant described above. If potentiometer A1R19 has been adjusted, apply glyptol.

3.3 ANTENNA (Model 8206) TEST PROCEDURE (Fig. 3-4)

1. Connect a length of coaxial cable to the output connector of a signal generator.

2. Wrap 2 turns of wire around the antenna. Connect one end of the wire to the coaxial cable shield. Connect the other side to a 1 K ohm resistor. The other side of the resistor is connected to the center conductor of the cable as shown in Figure 3-4.

3. Adjust the signal generator for an output of 60.000 KHz at 0.007 V RMS (0.014 volts behind 50-ohms).

4. Connect the output connector of the antenna to the oscilloscope as shown in the figure, with an 0.1 uf capacitor in series with the scope input.

5. Connect a 12 VDC power supply to the antenna output through a 27K ohm series resistor.

6. The oscilloscope shall display a 60.0 $\pm$.3 KHz resonant frequency at an amplitude of approximately 12 mV p-p and a bandwidth at the 3 dB points of approximately 800 Hz.

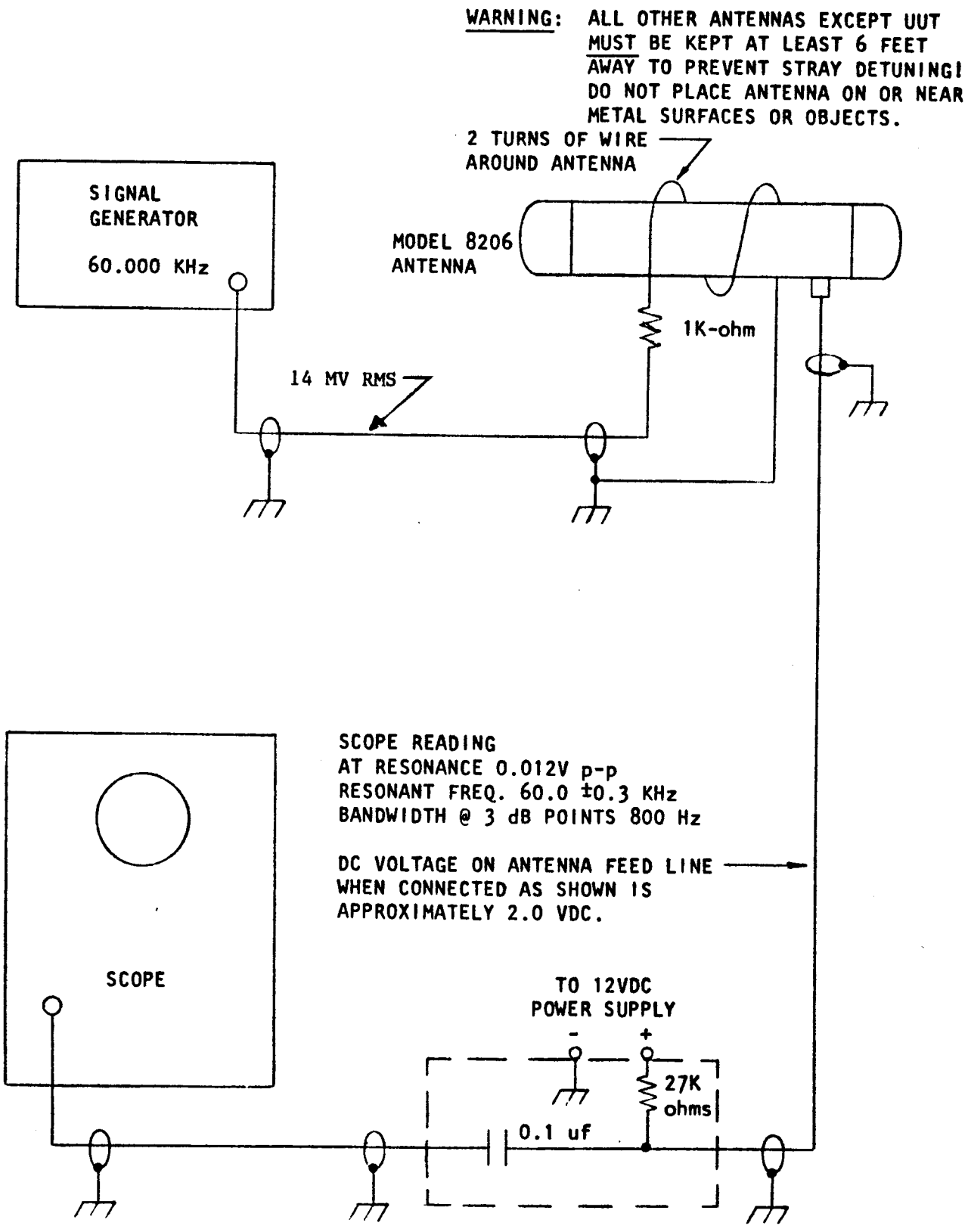


FIG. 3-4 ANTENNA MODEL 8206 TEST SETUP

3.4 MODEL 8207 - ANTENNA PREAMP ALIGNMENT
(requires an operating receiver)

1. Disconnect the receiver AGC wire (violet) from connector A1P2 by removing pin 6 from the connector. Be sure that pin 6 cannot make contact with any other circuits during the following tests, but leave the remaining wires in place and the connector mated with A2J5. Perform Receiver RF Amplifier Alignment Steps 2 through 8 only if not previously aligned.

2. Turn off the receiver and disconnect the signal generator. Connect the output of the antenna preamplifier to the receiver antenna input. Set receiver A1S1 to the preamp (right) position. Connect the signal generator output to a 40 dB pad. Connect the pad output to the preamp input through the network shown below.

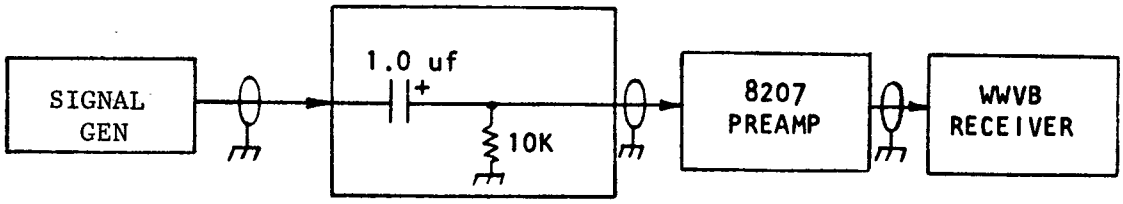


FIGURE 3-5 ANTENNA PREAMP ALIGNMENT SETUP

3. Align 8207 Preamp by performing RF Amplifier Alignment procedure steps 1 through 5. Adjust Preamp T1 instead of receiver A1T1.

4. Perform RF Amplifier Alignment procedure step 12.

5. Reconnect the violet wire on the receiver at A1P2-6.

NOTE: When performing this alignment, the Model 8207 preamp must be physically separated from the receiver by at least 10 feet using a long coaxial cable. Keep the cable from the signal generator to the preamp away from the vicinity of the receiver to prevent system regeneration.

3.5 TROUBLE SHOOTING

3.5.1 RECEIVER - If trouble occurs with a WWVB receiver, some simple checks can isolate the problem to specific areas of the receiver. Some of the more likely problems and the procedures for solving them are as follows:

1. RECEIVER DOES NOT LOCK. Improper reception. The most efficient way of solving this type of problem is to isolate the problem to one of the three major receiver system components. These are antenna, A1 RF Amplifier assembly, and A2 receiver board assembly.

A. Antenna DC check. Measure the DC voltage on the antenna line with a DVM. With the antenna connected to the receiver and the receiver turned on, the DC voltage on the coaxial line should be approximately +2.0 volts $\pm$ 10%. This can be measured by inserting a coaxial tee in the line at the rear of the receiver and measuring the antenna voltage with the antenna connected. With the antenna disconnected the DC voltage at the antenna terminal of the of the receiver should be approximately +11.5 volts DC $\pm$10%. If both these measurements are satisfactory, proper DC conditions are verified in both the antenna and its power supply in the receiver.

If the +11.5 volt level is not present with the antenna disconnected, the fault is in either the A1 RF amplifier assembly or in the A2 Receiver assembly. Disconnect the A1 board and check for +12 VDC at pin 1 of the connector A1P2. If the voltage is not present, the problem is in the power supply on the A2 board assembly (diodes CR12 through CR14, capacitors C53 through C57, or regulator U22). If the +12 volt level is present, the problem is in the A1 board assembly.

B. Check the receiver without the antenna connected. Using a signal generator set at 60.000 KHz with an accuracy of $\pm 1 \times 10^{-6}$, feed a 1.0 microvolt signal from the generator to the antenna input of the receiver and see if the receiver locks. If it does lock under this condition, the problem is most likely with the RF performance of the antenna or with the antenna placement or installation. If the receiver does not lock with 1.0 microvolt applied, the fault is in the receiver. Check the 60 KHz signal at E3 of RF amplifier board A1. If the signal is present, the RF amlifier is operating satisfactorily and the problem is in Receiver assembly board A2. If the 60 KHz signal is not

present at E3, the fault is in the A1 board assembly.

2. NO 1-MHZ NBS OUTPUT AT REAR PANEL JACK. Check pin 11 of U5A on A2 board to see that the oscillator stage containing A2Y1 is operating properly, and oscillating at 10.0 MHz. If this oscillator, which gets phase locked to WWVB, is not oscillating then the most likely problem is with the crystal Y1, which may need to be replaced. Another possibility is oscillator alignment. If this oscillator stage is not performing properly, the NBS output will not be present, and the receiver will not phase lock, or alternatively the phase lock lamp may remain on continuously even though the receiver is not operating properly. This condition can be checked by removing the antenna signal and checking to see that the phase lock lamp is extinguished after approximately 30 seconds. See section 3.2.2 paragraph 12 for instructions on oscillator alignment.

3. FUSE BLOWS. This problem is probably caused by power supply malfunction in the A2 board or in the chassis power supply components such as power transformers, filter capacitors, etc. The problem may be isolated to on or off-board causes by disconnecting all of the connectors from the A2 board and turning the unit on again. If the fuse still blows the cause is not on the A2 board. If the fuse does not blow with the connectors removed from the A2 board, reconnect them in the following order, turning power on after each connector is reattached:

A. Reattach the connector from the cable harness to A2J2. This connects the power transformers to the power supply rectifier circuits. If this causes the fuse to blow, the problem is probably a power supply short on the A2 board itself. Check the voltage regulators U21, U22, and U23 for proper operation. Check to see that Zener diode VR2 is not shorted to ground. This diode provides over-voltage protection on the +5 VDC line and will fuse, shorting to ground causing a fuse to blow if U21 fails and lets the +5 volts go high. Before replacing VR2, disconnect both VR2 and jumper W1 and check U21 for proper operation. If connecting the cable at A2J2 does not cause the fuse to blow after the power is reapplied, proceed to the next step.

B. Connect the A1 assembly to A2J5. Reapply power.

C. Connect the cable harness connector to A2J1. Reapply power. If this causes the fuse to blow, the problem is probably in the A3 or A4 assemblies.

D. Reconnect the cables at A2J3 and A2J4. A2J3 provides +5 volts DC to the other parts of the receiver, including the front panel and a short on one of these lines will cause a fuse to blow.

3.5.2 Microprocessor

1. VOLTAGE CHECKS - Measure the +5, +12, and -12 voltages at the microprocessor board. The +5 should be 4.75 to 5.25 volts. The ±12 should be nominal voltage ±1 volt.

   If the voltage is incorrect, check the power supply.

2. DIVIDER CHAIN - The 10 MHz signal from the receiver is divided down by U8, U14 and U15. Check the following pins for the proper signal:

   U8-14 - 10 MHz
   U8-11 - 1 MHz
   U14-10 - 200 Hz
   U14-17 - 1 Hz
   U15-1 - 10 KHz

3.6 MICROPROCESSOR AND DISPLAY ASSEMBLY

Figure 3-6 shows the component locations for the Display Board.

Figure 3-7 shows the component locations for the Microprocessor Assembly.

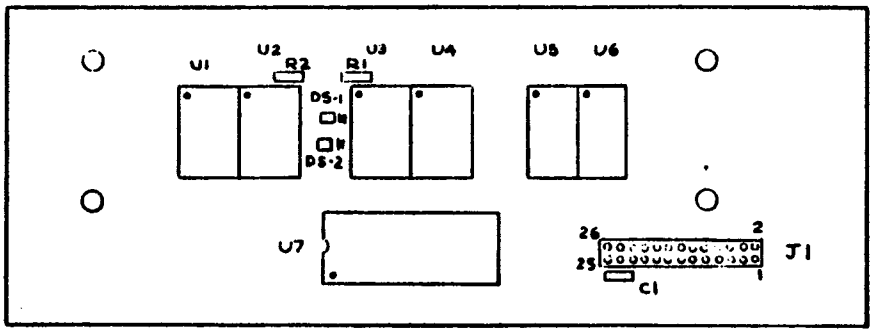


FIG. 3-6 ASSEMBLY DRAWING - DISPLAY BOARD A4

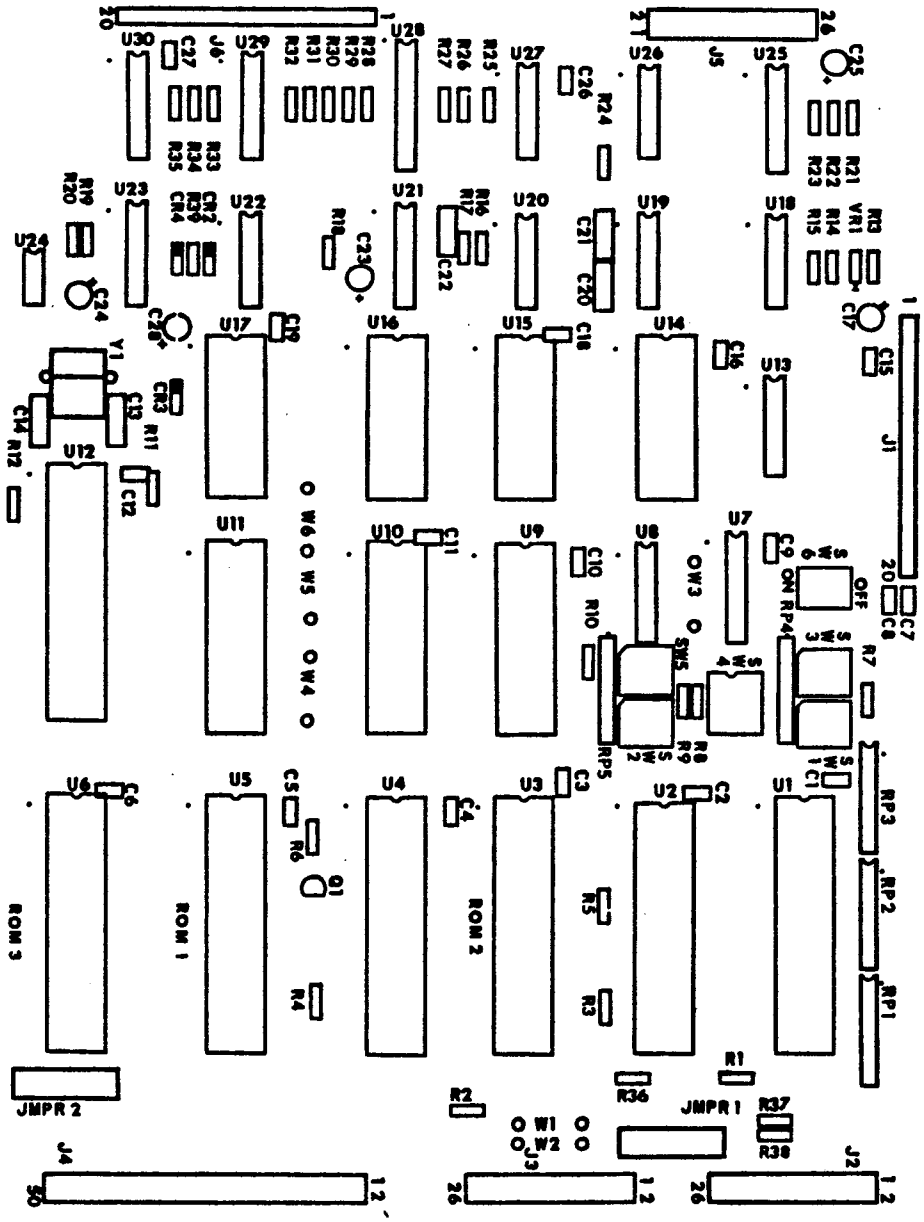


FIG. 3-7 ASSEMBLY DRAWING - MICROPROCESSOR A3

SECTION 4

MODEL 8170 OPTIONS

Option 15	-	Timing Pulse Outputs
Option 18	-	Parallel BCD Output
Option 19	-	Remote Output Driver
Option 23	-	IRIG B Output
Option 24,25	-	TCXO and External Oscillator Input
Option 28	-	1 KHz Output
Option 30	-	Fully Decoded Text Stream

4.1.0 OPTION 15 - TIMING PULSE OUTPUTS

Option 15 provides 60-Hz and 1-Hz TTL signals that are phase locked to the WWVB carrier. The 60-Hz signals is fed out on pin 49 of the rear panel 50-pin connector. The 1-Hz signal is fed out on pin 48. Pin 46 is ground for Option 15.

The signals are TTL-compatible square waves, each capable of driving a 93-ohm resistive load.

With normal signal reception the typical long-term timing accuracy is nominally 1×10^{-11}; short term accuracy is 1×10^{-5} typical.

4.1.1 OPTION 15 - PRINCIPLES OF OPERATION

The schematic for Option 15 is shown in Figure 4-1. The assembly drawing is shown in Figure 4-2.

The board is physically located between the front panel and assembly A2. The NBS 100 KHz input signal at A7J1-1 originates at A2J-12. It is divided by 5 by U1 and multiplied by 3 by the tripler. This 60-KHz signal is divided by 1000 by U2, U3, and U4 and the resulting 60-Hz signal is fed out by U7-8. Dividers U5 and U6 divide the 60-Hz signal by 60 and the 1-Hz signal is fed out on U7-6. These signals are wired to the rear panel 50-pin series D connector. The 60-Hz signal is on A5J6-49 and the 1-Hz signal is on A5J6-48. The ground return is pin A5J6-46.

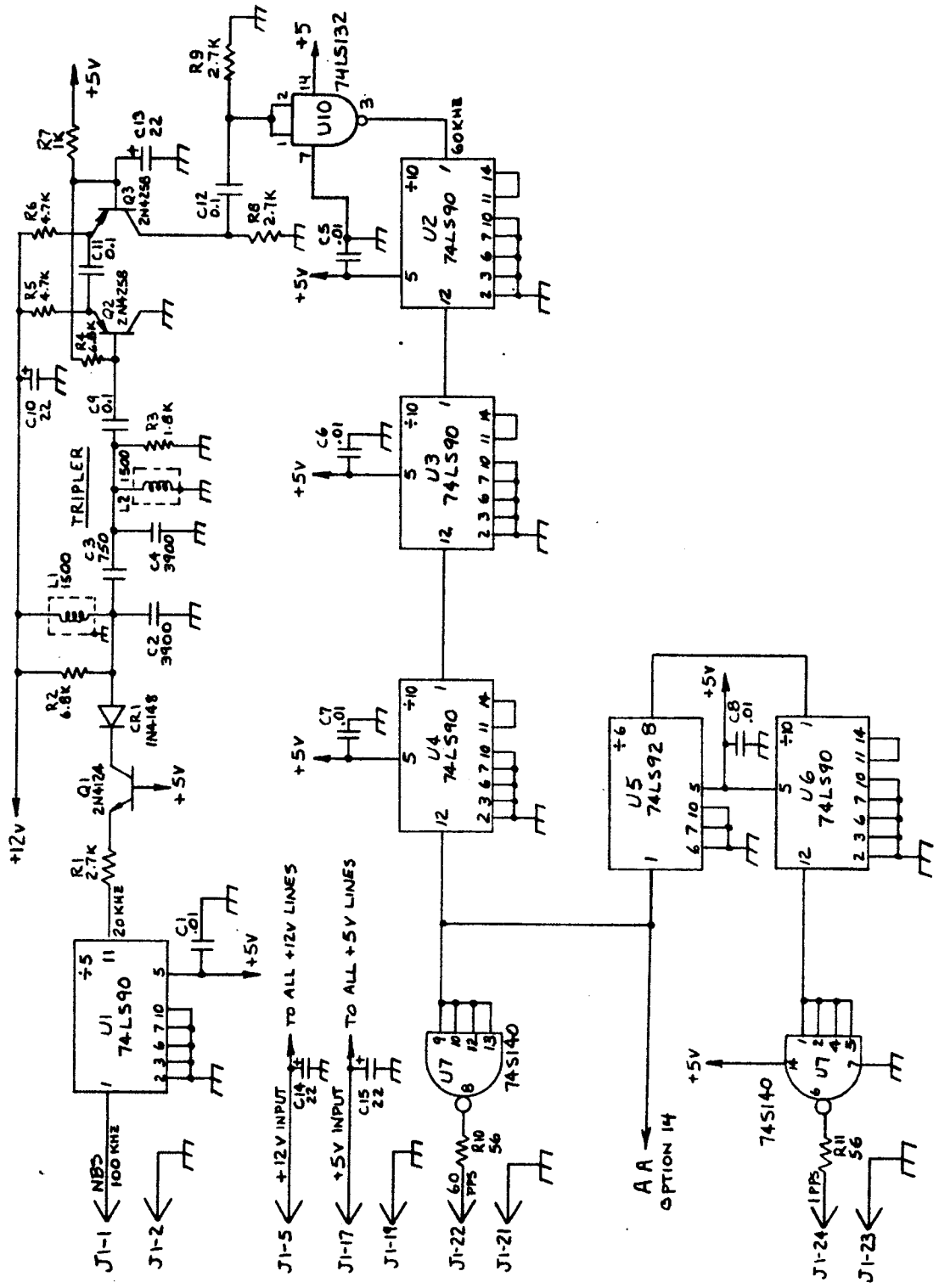


FIG. 4-1 OPTION 15 SCHEMATIC

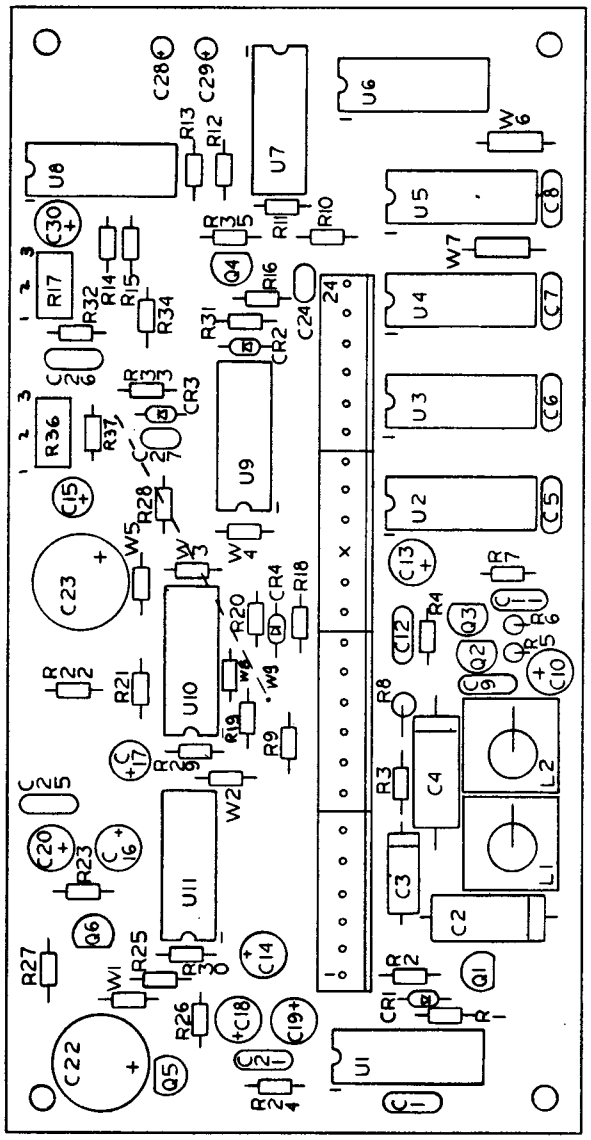


FIG. 4-2 OPTION 15 ASSEMBLY DRAWING

4.2.0 OPTION 18 - PARALLEL BCD OUTPUT

The Parallel BCD Option provides the day and time data in parallel BCD format on a 50-pin series D female connector (DD 50S). The connector is located on the rear panel. All lines are TTL-compatible and will drive one TTL load.

Data is valid 20 milliseconds before the ON-TIME pulse and remains valid until 850 milliseconds after the ON-TIME pulse.

All signals are positive logic: a logical 1 is a high, a logical 0 is a low.

The signal names and pin numbers are listed below. 8-4-2-1 BCD weighting is indicated in the mnemonic.

SIGNAL	MNEMONIC	PIN
Hours MSD	H8M	A5J6-1
"	H4M	A5J6-2
"	H2M	A5J6-3
"	H1M	A5J6-4
Hours LSD	H8L	A5J6-5
"	H4L	A5J6-6
"	H2L	A5J6-7
"	H1L	A5J6-8
Minutes MSD	M8M	A5J6-9
"	M4M	A5J6-10
"	M2M	A5J6-11
"	M1M	A5J6-12
Minutes LSD	M8L	A5J6-13
"	M4L	A5J6-14
"	M2L	A5J6-15
"	M1L	A5J6-16
Seconds MSD	S8M	A5J6-17
"	S4M	A5J6-18
"	S2M	A5J6-19
"	S1M	A5J6-20
Seconds LSD	S8L	A5J6-21
"	S4L	A5J6-22
"	S2L	A5J6-23
"	S1L	A5J6-24
Days MSD	D8M	A5J6-25
"	D4M	A5J6-26
"	D2M	A5J6-27
"	D1M	A5J6-28

SIGNAL	MNEMONIC	PIN
Days ISD	D8I	A5J6-29
"	D4I	A5J6-30
"	D2I	A5J6-31
"	D1I	A5J6-32
Days LSD	D8L	A5J6-33
"	D4L	A5J6-34
"	D2L	A5J6-35
"	D1L	A5J6-36
Time Zone MSD	TZ1M	A5J6-37
Time Zone LSD	TZ8L	A5J6-38
"	TZ4L	A5J6-39
"	TZ2L	A5J6-40
"	TZ1L	A5J6-41
Leap Year Switch	366	A5J6-42
Time Sync	Time Sync	A5J6-43
Ground	Gnd	A5J6-44
On-Time Pulse	1PPS	A5J6-45

The time data is valid when the TIME SYNC signal is high. The leading edge of the ON-TIME PULSE is the on-time point. The pulse has a 10% duty cycle.

4.2.1 OPTION 18 - PRINCIPLES OF OPERATION

The schematic for Option 18 is sheet 4 of Figure 2-6. The assembly drawing is Figure 3-7.

The HOURS, MINUTES and SECONDS are fed out by U4, a Programmable Peripheral Interface integrated circuit. The DAYS data are fed from U5.

Other signals brought out are:

366/365 - High if leap year switch is in position 366, otherwise low.

TIME SYNC - High if TIME SYNC LED on front panel is ON else it is low.

GND - Ground

1 PPS - The ON-TIME pulse that occurs once per second.

4.2.2 OPTION 18 - PERFORMANCE CHECKS

To verify the proper operation of Option 18, connect an RS-232C terminal to the Model 8170 WWVB Synchronized Clock. Adjust the TIME ZONE switch on the rear panel to zero.

Using the RS-232C terminal, manually set the clock to all 7's. The SET command is S777777777. This results in a BCD word for each digit of 0111. Verify that the output levels on the Option 18 Parallel BCD connector are proper.

Manually set the clock to all 8's. The SET command is S888888888. This results in a BCD word for each digit of 1000. Verify that this is true. Note that the seconds digits are changing, some interpolation is required for the seconds digits.

This test verifies that the DDD HH:MM:SS signals can be driven HIGH and LOW.

Check the levels of the TIME ZONE signals by first setting the TIME ZONE thumbwheel switch on the rear panel to 07 and measure the outputs, then setting the switch to 18 and measure the outputs for proper value.

Install the Model 8206 antenna and Model 8170 WWVB Synchronized Clock. Before the clock sets, observe that the TIME SYNC signal out of the Option 18 connector is LOW. Obtain TIME SYNC. Observe that the TIME SYNC signal goes HIGH.

Check the ON-TIME pulse. Monitor with an oscilloscope and observe that it is a TTL signal that occurs once per second and has a 10% duty cycle. The leading edge is the ON-TIME point.

4.3.0 OPTION 19 - REMOTE OUTPUT DRIVER

Standard on units with serial number 601 and above.

The Spectracom Model 8170 WWVB Synchronized Clock receives and decodes the time signal transmitted by the National Bureau of Standards at Ft. Collins, Colorado. Option 19 Remote Output Driver provides a method of distributing this data to multiple remote locations. Once-per-second a string of ASCII characters that contain day-of-year, time-of-day, and time zone setting information are sent on the bus. An on-time pulse and a time sync status signal is also transmitted. The electrical characteristics of the data signals conform to the EIA RS-422 standard. Up to 32 receivers may be employed at distances up to 4000 feet.

If Option 30, Fully Decoded Text Stream, is present, the day of the week, month and year are transmitted. The day of the year (1-366) and TIME ZONE switch setting is not transmitted.

The Spectracom Model 8173 Multiple RS-232C Tap may be connected to the Remote Output bus. Model 8173 provides four RS-232C ports for easy interfacing to computer systems. Up to 32 Model 8173's may be connected to the bus.

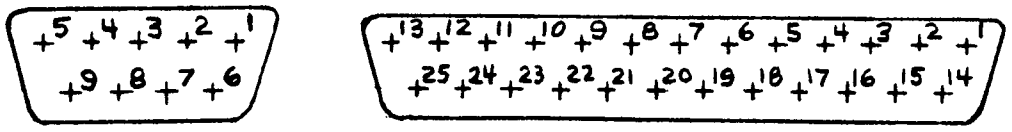
An unlimited number of ports may be obtained by using the buffered output bus on the Model 8173. This port regenerates the data and provides another set of RS-422 drivers that can drive up to 32 loads at 4000 feet.

The Spectracom Model 8172 Remote Clock may be connected to Option 19 Remote Output Driver. Model 8172 is a digital wall clock that provides an HOURS, MINUTES, SECONDS 12- or 24-hour display.

The time data are also brought out as an RS-232C signal on both the Remote Output connector pin 5 and the Serial ASCII connector pin 19.

4.3.1 OPTION 19 - SPECIFICATIONS

Output Connector - The Remote Output Connector is a 9-pin series D receptacle (female). The Serial ASCII output connector is a 25-pin series D receptacle. Figure 4-3 shows the pin locations viewed from the rear of the Model 8170.



A5J7 A5J5

FIGURE 4-3 REMOTE CONNECTOR AND SERIAL ASCII CONNECTOR

SIGNAL	MNEMONIC	CONNECTOR PIN	SERIAL ASCII CONNECTOR PIN
BUS DATA	-BDATA	A5J7-3	
BUS DATA	+BDATA	-8	
BUS ON-TIME	-BON-TIME	A5J7-2	
BUS ON-TIME	+BON-TIME	-7	
BUS TIME SYNC	-BTSYNC	A5J7-1	
BUS TIME SYNC	+BTSYNC	-6	
ENABLE	ENABLE	A5J7-4	
GROUND	GND	-9	
TIME DATA	TDATA	A5J7-5	A5J5-19

BDATA, BON-TINE and BTSYNC signals conform to EIA RS-422 standard. TDATA conforms to RS-232C signal levels.

The +BON-TIME signal is a positive-going 0.1-second pulse relative to -BON-TIME, occuring once per second. The leading edge of the pulse is the beginning of the second.

The +BTSYNC signal is high relative to -BTSYNC after the NBS time code has been decoded. The signal goes low n minutes after the receiver has lost phase lock with the NBS signal. The number of minutes, n, that the signal stays active after the receiver has lost phase lock is selected by switch A3SW4-3,4. It remains low until another successful decoding is accomplished.

The ENABLE signal is +5 volts in series with 60 ohms.

Time information is broadcast in ASCII on BDATA and TDATA. A character consists of 1 start, 8 data, and 2 stop bits. Serial Data Structure is:

(CR)(LF)I(SPACE)(SPACE)DDD(SPACE)HH:MM:SS(SPACE)(SPACE)TZ=XX(CR)(LF)

where: I = space if clock set by WWVB (TIME SYNC lamp on)
* if clock set manually via RS-232 port
? if time sync lamp is off

DDD - Day of the year
HH:MM:SS = hours:minutes:seconds
XX = Time zone switch setting at rear panel

Output is UTC minus the time zone switch setting

Option 30 Fully Decoded Text Stream: This alternate data format can be furnished when the unit is purchased.

(CR)(LF)I(SPACE)WWW(SPACE)DDMMMYY(SPACE)HH:MM:SS(CR)(LF)

where: I = as defined above
WWW = day of week (MON, TUE, WED, etc.)
DD = numeric day of month (01 to 31)
MMM = month (JAN, FEB, MAR, APR, etc.)
YY= year without century (83, 84, 85, etc.)
HH:MM:SS = as defined above.

BUS IMPEDANCE - The source impedance is 120 ohms. At the far end of the bus terminate BDATA, BON-TIME, BTSYNC with 120 ohms connected across each twisted pair. Spectracom Bus Terminator part No. 016005 may be used.

CABLE - Twisted pair cable should be used for each of the signals.

4.3.2 OPTION 19 - PRINCIPLES OF OPERATION

This section discusses the circuits associated with Option 19, Remote Output Driver. The Schematic for the microprocessor board is shown in Figure 2-6 Sheet 2. Figure 3-7 is the parts location drawing for the microprocessor board.

Option 19 adds a USART and a RS-422 driver to the microprocessor board. Day and time information is broadcast out once per second.

The on-time pulse IRO, interrupts the processor once per second. During this interrupt the processor initiates the transmission of time data to the USART. The USART performs a parallel/serial conversion and broadcasts the data on to the time bus via the RS-422 driver, U29 and RS-232C driver U19.

The first character, carriage return, follows the on-time pulse by less than 10 msec. The standard baud rate is 300. Higher baud rates may be selected by the Selectable Bit Rate switch A3SW2. Baud rates lower than 300 are too slow for the amount of data transmitted.

The Model 8170 1PPS ON-TIME pulse is transmitted on the RS-422 time bus. This signal comes from A3U27-8 and is sent down the bus by A3U29. The signal is a positive-going once-per-second 100-millisecond pulse. It is synchronized to the on-time signal received from WWVB minus the setting of the path delay thumbwheel switch that is located on the rear panel.

The TIME-SYNC indicator is transmitted on the bus via A3U29. The signal will be high when the indicator is on and low when the indicator is off.

An ENABLE signal A3J6-7 comes from +5 volts through 60 ohms. Devices on the time bus may use this signal to enable their RS-422 receivers.

Ground is brought out on A3J6-8.

In summary, the processor is interrupted once-per-second by the on-time pulse. This initiates the transmission of the time data on the RS-422 bus and the RS-232C output. Other signals transmitted are the on-time pulse, time sync indicator, and enable signal.

4.3.3 OPTION 19 - PERFORMANCE CHECKS

This section contains maintenance information for Option 19. The test equipment required is an oscilloscope, a Spectracom Model 8173, and an RS-232C terminal.

TEST 1 - BDATA

Connect an RS-232C terminal to the Remote Output via the Model 8173 or connect an RS-422 terminal directly to the Remote Output bus. The terminal will print/display the day of the year and time of day once per second.

If Option 30 is present, the day format will contain day of week, month, and year data.

TEST 2 - BON-TIME

Using the oscilloscope observe the differential voltage between pin 7 and pin 2 on the Remote connector. The signal is a once-per-second 100-millisecond positive-going pulse greater than +2 volts in amplitude.

TEST 3 - BTSYNC

On the Remote connector, observe the differential voltage between pin 6 and pin 1. When the Model 8170 Time Sync LED on the front panel is on, the differential voltage should be greater than +2 volts. When the Time Sync LED is off the voltage on pin 6 should be negative relative to pin 1 by a minimum of 2 volts.

TEST 4 - ENABLE

With power on, the voltage at pin 4 should be +5 $\pm$0.5 volts.

TEST 5 - TDATA

Monitor the TDATA output on pin 5 Remote output connector. The serial stream of data should be greater than $\pm$9 volts above and below ground. Monitor the same signal at pin 19 of the Serial ASCII connector.

These tests verify the proper operation of Option 19. If trouble is found, trace the signal back to the faulty IC, connector or component. Repair/replace and retest.

4.4.0 OPTION 23 - IRIG B OUTPUT

IRIG Option 23 provides the Spectracom Model 8170 WWVB Synchronized clock with an IRIG B Output. Both the BCD time code and Straight Binary Seconds, SBS, time code are provided.

If Option 18, Parallel BCD is also present, then the IRIG control functions, CF, is provided. The input CF and output parallel BCD function share the same connector. An internal switch selects the CF INPUT function or the OUTPUT function. When shipped from the factory, the switch is in the CF INPUT position.

The control function capability is present only on units equipped with both Option 18 Parallel BCD Output and Option 23, IRIB B Output.

Refer to Document 104-70 IRIG STANDARD TIME FORMATS published by the Range Commander's Council, White Sands Missile Range, August 1970 for details on the IRIG STANDARD TIME FORMATS.

4.4.1 OPTION 23 - SPECIFICATIONS

IRIG OUTPUTS: The IRIG code is brought out a rear panel BNC connector. The output is a TTL signal or an amplitude modulated signal. The selection is made by an internal switch.

TTL OUTPUT: TTL 50-ohm line driver (SN74S140).

AMPLITUDE MODULATED OUTPUT: A 1-KHz sine wave amplitude modulated by the time code. The open circuit output signal is a nominal:

MARK: 8 volts peak-to-peak
SPACE: 2.4 volts peak-to-peak

The output impedance is nominally 50 ohms and will drive a load of 600 ohms to ground.

PARALLEL INPUT/OUTPUT: If Option 18 is present, then the 50-pin series D receptacle on the rear panel may be an INPUT for CONTROL FUNCTIONS or an OUTPUT for parallel BCD time-of-year data. The selection is made by internal switch A3SW4-1. If CLOSED ("1") data is read in and encoded in the control function field of the IRIG message. Figure 4-4 shows the receptacle as viewed looking at the rear panel.

FIGURE 4-4 50-PIN SERIES D RECEPTACLE

PARALLEL BCD OUTPUT: In the parallel BCD output mode all signals are TTL-compatible and will drive one TTL load. Data are valid 20 milliseconds before the ON-TIME pulse and remains valid until 850 msec after the ON-TIME pulse.

All signals are positive logic: a logical 1 is high, a logical 0 is low.

The clock will not provide output data until it has been set by WWVB or by the SET command.

CONTROL FUNCTONS INPUT: In the control Functions (CF) mode, data are input to the 50-pin connector and encoded into the IRIG B data stream. The inputs are sampled at the ON-TIME point ±2 milliseconds. The requirements for the INPUT signal levels are:

INPUT LOW VOLTAGE	-0.5 TO 0.8 volts
INPUT HIGH VOLTAGE	2.0 to 5.0 volts

The input load current is a maximum of ±10 microamperes.

The signal names and pin numbers are listed below:

SIGNAL	MNEMONIC	PIN	CONTROL FUNCTION ELEMENT
Hours MSD	H8M	A5J6-1	16
''	H4M	A5J6-2	15
''	H2M	A5J6-3	14
''	H1M	A5J6-4	13

SIGNAL	MNEMONIC	PIN	CONTROL FUNCTION ELEMENT
Hours LSD	H8L	A5J6-5	12
''	H4L	A5J6-6	11
''	H2L	A5J6-7	10
''	H1L	A5J6-8	9
Minutes MSD	M8M	A5J6-9	24
''	M4M	A5J6-10	23
''	M2M	A5J6-11	22
''	M1M	A5J6-12	21
Minutes LSD	M8L	A5J6-13	20
''	M4L	A5J6-14	19
''	M2L	A5J6-15	18
''	M1L	A5J6-16	17
Seconds MSD	S8M	A5J6-17	8
''	S4M	A5J6-18	7
''	S2M	A5J6-19	6*
''	S1M	A5J6-20	5
Seconds LSD	S8L	A5J6-21	4
''	S4L	A5J6-22	3
''	S2L	A5J6-23	2
''	S1L	A5J6-24	1
Days MSD	D8M	A5J6-25	
''	D4M	A5J6-26	
''	D2M	A5J6-27	
''	D1M	A5J6-28	
Days ISD	D8I	A5J6-29	
''	D4I	A5J6-30	
''	D2I	A5J6-31	
''	D1I	A5J6-32	
Days LSD	D8L	A5J6-33	
''	D4L	A5J6-34	
''	D2L	A5J6-35	
''	D1L	A5J6-36	
Time Zone MSD	TZ1M	A5J6-37	
Time Zone LSD	TZ8L	A5J6-38	
''	TZ4L	A5J6-39	
''	TZ2L	A5J6-40	
''	5Z1L	A5J6-41	
Leap year Switch	366	A5J6-42	
Time Sync	Time Sync	A5J6-43	
Ground	Gnd	A5J6-44	
On-Time Pulse	1PPS	A5J6-45	

*CONTROL FUNCTION ELEMENT 6 is used to indicate the status of the TIME SYNC LED. A logical 1 indicates time sync, a logical 0 indicates that the TIME SYNC LED is off.

4.4.2 OPTION 23 - INTERNAL SWITCHES

There are two internal dip switches associated with the IRIG option. Refer to the layout drawing Figure 3-7 for the physical location of the switches on the microprocessor board.

Switch A3SW4-1 is the CF switch. It controls the direction of data TO/FROM the rear panel Parallel BCD connector. This switch is functional when IRIG Option 23 and Parallel BCD Option 18 are present.

With the switch in the ON position, Control Function (CF) data is read into the Model 8170. With the switch in the OFF position, parallel BCD time-of-year data is read out of the Model 8170.

W A R N I N G

DO NOT APPLY INPUT DATA TO THE PARALLEL CONNECTOR WHEN THE SWITCH A3SW4-1 IS IN THE PARALLEL BCD POSITION. THIS COULD CAUSE DAMAGE TO U4 OR U5.

Switch A3SW6 TTL/AM, controls the signal applied to the IRIG output. In the TTL or ON position, the output signal is a TTL level. In the AM or off position, the signal is an amplitude modulated 1-KHz signal.

4.4.3 OPTION 23 - PRINCIPLES OF OPERATION

Figure 2-6 Sheet 5 is the schematic for the IRIG option. Figure 3-7 is the layout drawing for the microprocessor assembly A3.

The first section that will be described is the counter chain. The chain consists of 5 counters. Counter 0 in U17 divides the 1-MHz input on U17-9 by 10 and provides a 100-KHz output on U17-10. This signal is fed into counter 1 and 2 on pins U17-15 and U17-18. Counter 1 divides the 100 KHz input by 1000 to produce the frame element signal F_E (100 Hz). This signal interrupts the processor and causes the processor to output the next element to counter 2.

Counter 2 is programmed as a ONE-SHOT. The output at U17-17 drops at the beginning of the framing element and stays low for a period of 2, 5, or 8 milliseconds. This signal is inverted and amplified by U13, a 50-ohm TTL line driver. The signal is fed to the rear panel IRIG BNC connector via the TTL/AM select switch.

Counter 0 of U16 divides the 1 MHz input signal at U16-9 by 1000 to obtain the 1000-HZ carrier frequency at U16-10.

Counter 1 of U16 divides the 1-MHz input signal, U16-15 by 20 to obtain the 50-KHz clock frequency for the switched capacitor low pass filter U28.

The signals are synchronized to the ON-TIME pulse by U21, a one-shot. The output signal U21-4 is a negative-going 400 nanosecond pulse that is used to reset counters 0 and 1 of U17 and counter 0 of U16.

The output from counter 0 of U16 is a 1-KHz square wave. It is filtered by U28, a 4th order low pass switched-capacitor filter. The output from the filter is fed into the amplitude modulator. The modulator consists of operational amplifier U18 and analog switch U25. The analog switch is a single-pole double-throw switch which is controlled by the IRIG code. Feedback resistors R21 and R22 are selected by the switch. The output of the modulator is buffered by voltage follower U18 and fed to the rear panel IRIG BNC connector via a 51 ohm resistor and the TTL/AM select switch.

The code select switch in the lower left of the schematic selects the IRIG B code. The other positions are reserved for future code options. The outputs from the code select switch are fed to the processor via U3 Port B.

4.4.4 OPTION 23 - PERFORMANCE CHECKS

This section describes verification tests for Option 23.

Table 4-1 lists the recommended test equipment for checking the operation of the IRIG Option.

TABLE 4-1 RECOMMENDED TEST EQUIPMENT

INSTRUMENT	REQUIRED CHARACTERISTICS	RECOMMENDED
Oscilloscope	2 Channel	Tektronix Model 455
Time Code Reader	Read IRIG B Code	Datum Systron-Donner

The test set-up is shown in Figure 4-5.

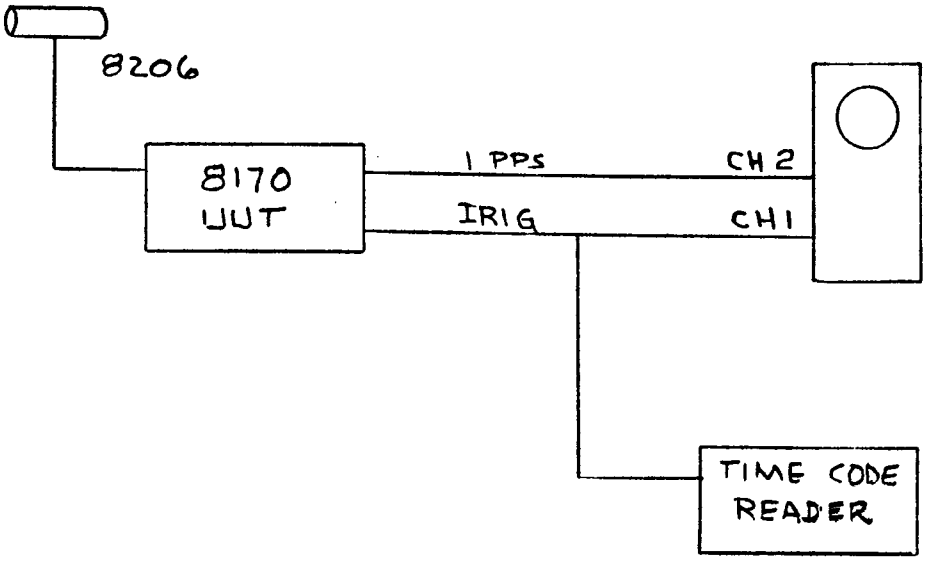


FIGURE 4-5 IRIG TEST SET-UP

Connect the Model 8170 WWVB Synchronized Clock to the Model 8206 antenna and achieve Time Sync. Connect the IRIG output to channel 1 of a dual trace oscilloscope such as a Tektronix 455. Connect the 1 PPS output to channel 2. Synchronize the sweep to channel 2, 1 PPS and view the IRIG code on channel 1.

Connect an IRIG B Time Code Reader to the IRIG output. If control functions are present connect the CF inputs.

PERFORMANCE TESTS:

A. IRIG AM OUTPUT - With the TTL/AM switch A3SW6 in the OFF position, the output signal will be an amplitude modulated signal. The carrier frequency is 1 KHz and the mark to space ratio is typically 3.3 to 1.

V OUT MARK (7.2 - 9.0 V P-P) _____volts
V OUT SPACE (2.1 - 2.8 V P-P) _____volts

B. IRIG TTL OUTPUT - With the TTL/AM switch A3SW6 in the ON position, measure the IRIG TTL output signals.

V OUT HIGH (>2.7 volts) _____volts
V OUT LOW (<0.5 volts) _____volts

C. IRIG CODE WORD - Set the TTL/AM switch, A3SW6, to the ON position (TTL). Set the sweep speed at 5 milliseconds per division and synchronize the scope with the 1 PPS ON-TIME pulse. The scope will display the first 5 elements of the IRIG Code Word. The first element is 8 milliseconds in duration, the subsequent elements represent the least significant seconds bits.

Pulses will be 2 or 5 milliseconds wide.

Position Identifier (8 msec) _____
Weighted Code Digit (5 msec) _____
Unweighted Code Digit (2 msec) _____

D. READING THE TIME CODE - Connect a time code reader to the IRIG output. Verify that the BCD and SBS Code Words are correct.

BCD Code Word _____
SBS Code Word _____

E. CONTROL FUNCTIONS - If Option 18 is present, the CONTROL FUNCTIONS may be brought into the rear panel 50 pin series D receptacle. This data will be encoded into the IRIG B data. Set the CF switch, A3SW4-1, in the ON position. Test that each control function can be encoded low and high. Note that control function element 6 is reserved for TIME SYNC stations and therefore not available.

Control Functions _____

4.5.0 OPTION 24 AND 25 - TCXO AND EXTERNAL OSCILLATOR INPUT

Option 24 - Standby TCXO. A temperature compensated crystal oscillator provides the time base to the clock during signal loss, improving time error accumulation from about 1 second per day to about 0.01 seconds per day. Option 25 is included as part of Option 24.

Option 25 - External Oscillator Input. Rear panel BNC input for 1.0 MHz standby clock oscillator. Maintains improved accuracy during signal loss.

4.5.1 OPTION 24 AND 25 - SPECIFICATIONS

EXT 1-MHZ INPUT: This signal is AC coupled into 100-ohm terminating resistor. The signal level shall be a minimum of 1 V peak-to-peak and a maximum of 10 V peak-to-peak. A BNC connector is used.

TEMPERATURE-COMPENSATED CRYSTAL OSCILLATOR, TCXO: (Option 24 only).

Temperature Stability 0°C to 50°C: $\pm 1 \times 10^{-6}$

Aging Rate: 5×10^{-7}/year, 3×10^{-9}/day average

Short-term stability 1×10^{-9}/second under constant conditions.

Frequency Adjustment: Sufficient to compensate for 5 to 10 years of aging.

Adjustment Resolution: $< 1 \times 10^{-7}$

Accuracy: Set at the factory to $\pm 1 \times 10^{-7}$

4.5.2 OPTION 24 AND 25 - PRINCIPLES OF OPERATION

The time base for the Model 8170 WWVB Synchronized clock is normally derived from a voltage-controlled oscillator that is phase locked to the WWVB signal.

Options 24 and 25 provide a TCXO or external oscillator for the clock when the WWVB Signal is not present. Without these options the 8170 time base will be the voltage-controlled crystal oscillator on assembly A2.

Figure 4-6 is the schematic for Options 24 and 25. The data selector U2, chooses the appropriate 1 MHz to be the time base for the clock. The truth table on the schematic shows which one is selected: If the receiver is phase locked to WWVB, the VCXO oscillator from A2 is selected. If the receiver is not phase locked to WWVB, the time base selected will be the External 1-MHz Input, if present. If there

is no External Input, the TCXO will be selected if present. If neither an External Input nor a TCXO is present, the VCXO time base is selected.

The impedance of the External 1-MHz Input is 100 ohms (R3). RS-422 receiver U3 amplifies and translates the signal to TTL levels. The signal is DC-restored to ground by C6-R1-CR1. The External 1-MHz signal is applied to pins 1 and 2 of the data selector U2 and amplifier U4. Level detector CR2-C7 senses the 1 MHz if present. The level is buffered by U4 and applied as a control input to the data selector U2-10.

The 1-MHz output of the data selector is fed to connector pin J1-12 on the microprocessor board A3. When Option 24/25 is NOT installed, this signal is the 10 MHz from the A2 VCXO, which is then divided by 10 in A3U8. When Option 24/25 is installed, A3U8 is deleted and W3 is inserted in its place to feed 1 MHz directly to A3U14.

Figure 4-7 shows the component locations for the Option 24/25 board.

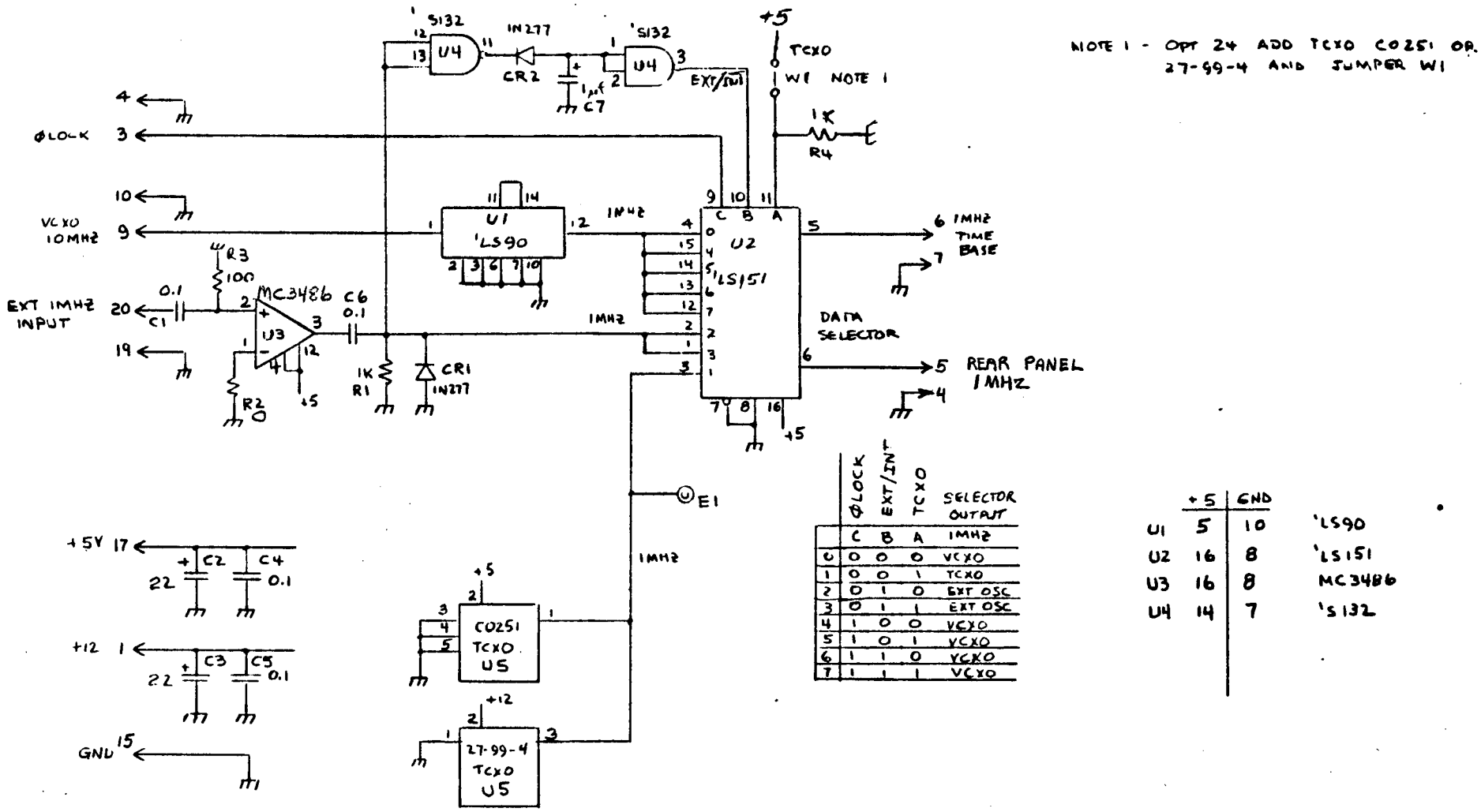


FIG. 4-6 OPTION 24 AND 25 SCHEMATIC

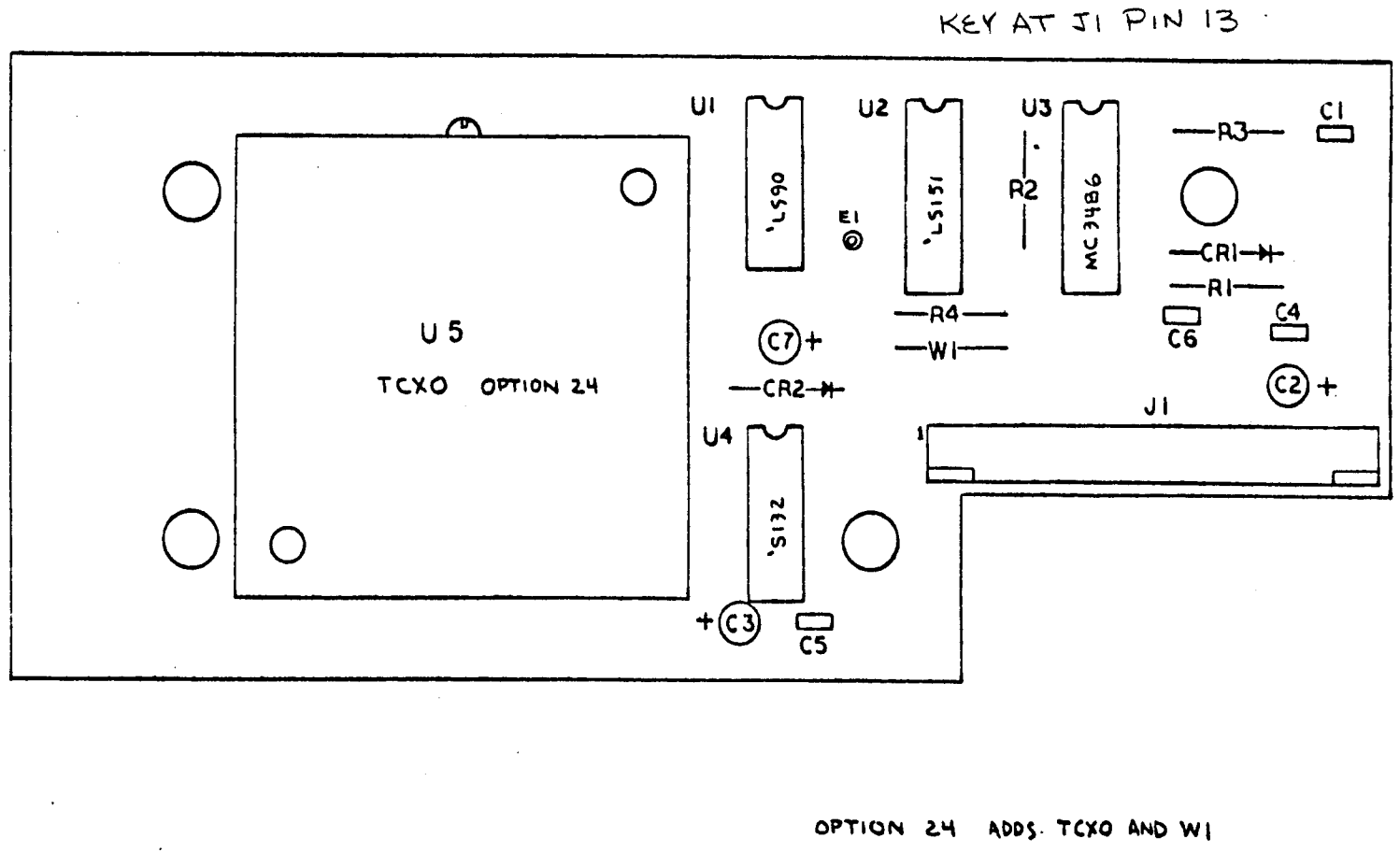


FIG. 4-7 OPTION 24/25 ASSEMBLY DRAWING

4.5.3 OPTION 24 AND 25 - PERFORMANCE CHECKS

This section describes how to verify the proper operation of Option 24/25.

4.5.3.1 TEST EQUIPMENT

Table 4-2 lists the recommended test equipment for checking the performance of Option 24/25.

Test equipment with equivalent characteristics may be substituted.

TABLE 4-2 RECOMMENDED TEST EQUIPMENT

INSTRUMENT	REQUIRED CHARACTERISTICS	RECOMMENDED
STANDARD OSCILLATOR	1 MHZ with an accuracy of $\pm 1 \times 10^{-8}$ and a minimum output of 1 V peak-to-peak into 100 ohms.	SPECTRACOM Model 8131
OSCILLOSCOPE	2-channel	Tektronix Model 455
ATTENUATER	50 ohms	
PHASE COMPARATOR	Measure frequency difference to 1×10^{-8}.	SPECTRACOM Model 8150

4.5.3.2 TEST PURPOSE

The purpose of these tests is to verify that the data selector A8U2 on the Option 24/25 board is selecting the desired 1-MHz time base. The truth table below identifies the data selector output as a function of the phase lock signal and the External 1-MHz signal.

PHASE LOCK	EXT 1-MHZ INPUT	1-MHZ SELECTOR OUTPUT (A3U5-9)
0	0	TCXO - Op. 24 VCXO - Op. 25
0	1	EXT 1 MHz INPUT
1	0	VCXO
1	1	VCXO

4.5.3.3 OPTION 24 AND 25 TEST SET-UP

Figure 4-8 illustrates the test set up.

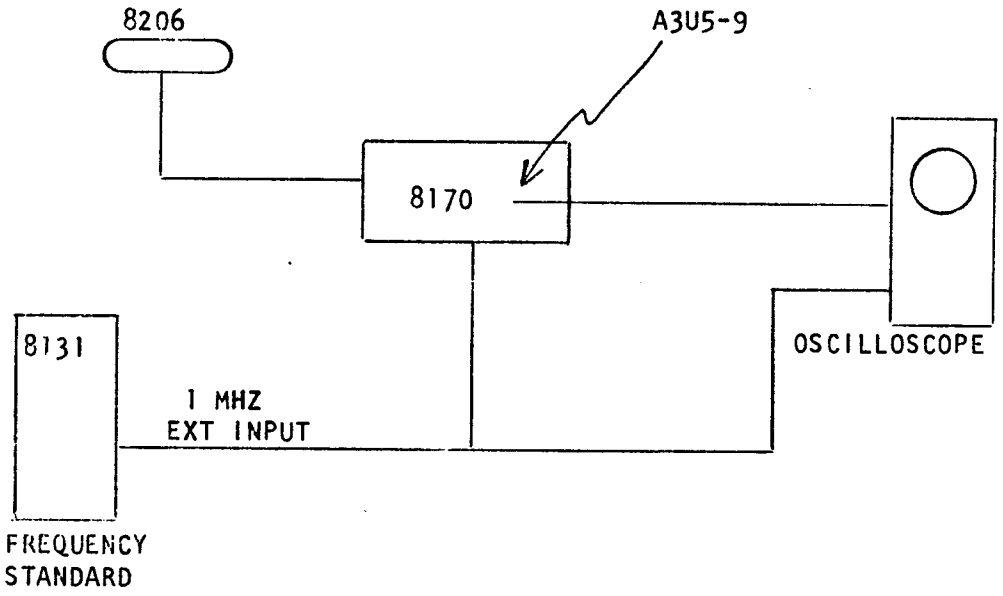


FIGURE 4-8 OPTION 24 AND 25 TEST SET-UP

Connect a 1-MHz standard signal to the EXT 1-MHz INPUT on the rear of the 8170, and to Channel A of the oscilloscope. Verify that the 1-MHz signal amplitude is equal to or greater than 1 volt peak-to-peak.

Remove the top cover of the 8170. Attach a "dip clip" to A3U14. Connect Channel B of the oscilloscope to A3U14. This signal is the output of data selector A8U2.

Connect the antenna to the 8170 and apply power.

Observe that the front panel LOCK light comes on and the display is incrementing.

4.5.3.4 OPTION 24 AND 25 TEST PROCEDURE

TEST 1 - VCXO SELECTED

With the 8170 phase locked to WWVB the signal at A3U14 will be 1.0 MHz from the receiver VCXO.

This signal is on Channel B of the scope. It is a 1-MHz signal with a 1-3 microsecond jitter. The jitter is a function of the signal-to-noise ratio received at the antenna.

TEST 2 - EXT 1-MHZ SELECTED

Remove the antenna. After 30 seconds the LOCK light will go off and the UNLOCK light will come on. The signal at A3U14-9 will be the EXT 1-MHZ INPUT.

This can be identified because it does not have jitter or drift with respect to the signal on Channel A. It is derived from the Channel A signal.

TEST 3 - TCXO SELECTED

Remove the EXT 1-MHZ INPUT from the 8710. The signal at A3U14-9 will be the TCXO 1 MHz if Option 24 is present. Otherwise, it will be the VCXO signal. The TCXO signal can be identified by its slow drift relative to the signal on Channel A.

A drift of 1 microsecond in 10 seconds corresponds to a frequency offset from the 1-MHz standard of 1×10^{-7}.

TEST 4 - INPUT SENSITIVITY

Connect a 50-ohm attenuator between the 1-MHz standard and the EXT 1-MHZ INPUT connector on the rear panel.

Adjust the attenuator for a 1 volt peak-to-peak output. Observe A8U2-1 for a TTL square wave.

TEST 5 - TCXO FREQUENCY ADJUST (Option 24)

Connect the 1-MHz Frequency Standard to REF INPUT of the Spectracom Model 8150. Connect the output form the TCXO (Test Point E1 or A8U2-3) to the LOCAL INPUT. Depress the N-1 switch on the Model 8150 and measure the frequency offset.

Remove the screw on top of the TCXO on A8 and adjust the oscillator to within 1×10^{-7} of the desired 1 MHz. Replace the screw.

This completes the Option 24/25 tests.

4.6.0 OPTION 28 - 1 KHZ OUTPUT

This option provides a 1-KHz signal that is phase locked to the WWVB carrier. The signal is a TTL-compatible 3.4 volt square wave. It will drive a 93-ohm resistive load. It is brought out on pin 47 of the rear panel 50-pin connector. Pin 50 is Option 28 ground.

The typical long term timing accuracy with normal signal reception is 1×10^{-11}, short term accuracy is nominally 1×10^{-5} or better.

4.6.1 OPTION 28 - PRINCIPLES OF OPERATION

The schematic for Option 28 is shown in Figure 4-9. The assembly drawing is Figure 4-10. The board is physically located between the front panel and the A2 board.

The NBS 100 KHz from A2J4-10 is fed into U5-1, where it is divided by 10. This 10-KHz signal is fed into U4-1 and divided down to 1 KHz. Buffer amplifier U3 feeds the signal to the rear panel 50-pin series D connector pin 47.

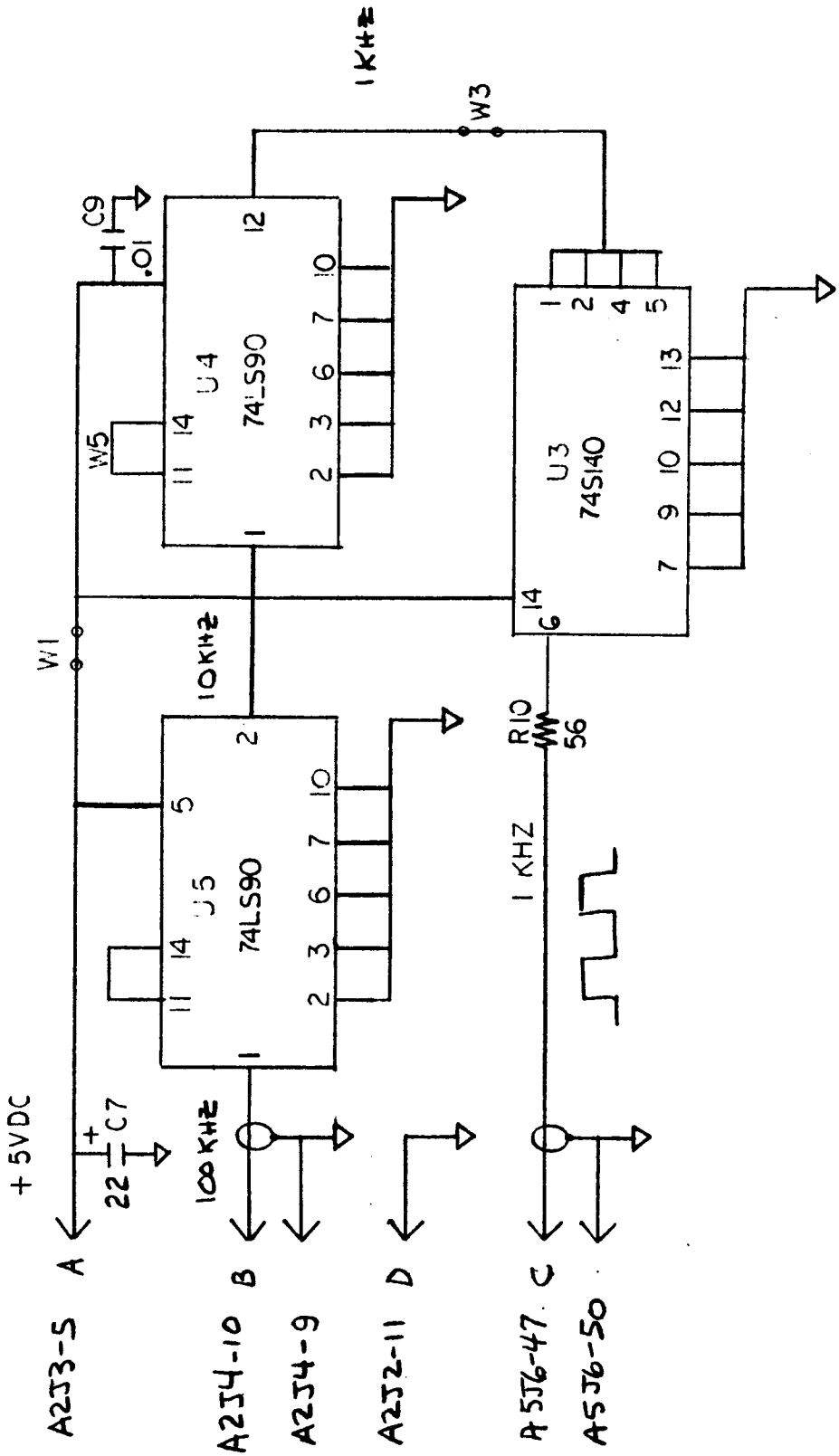


FIG. 4-9 OPTION 28 SCHEMATIC

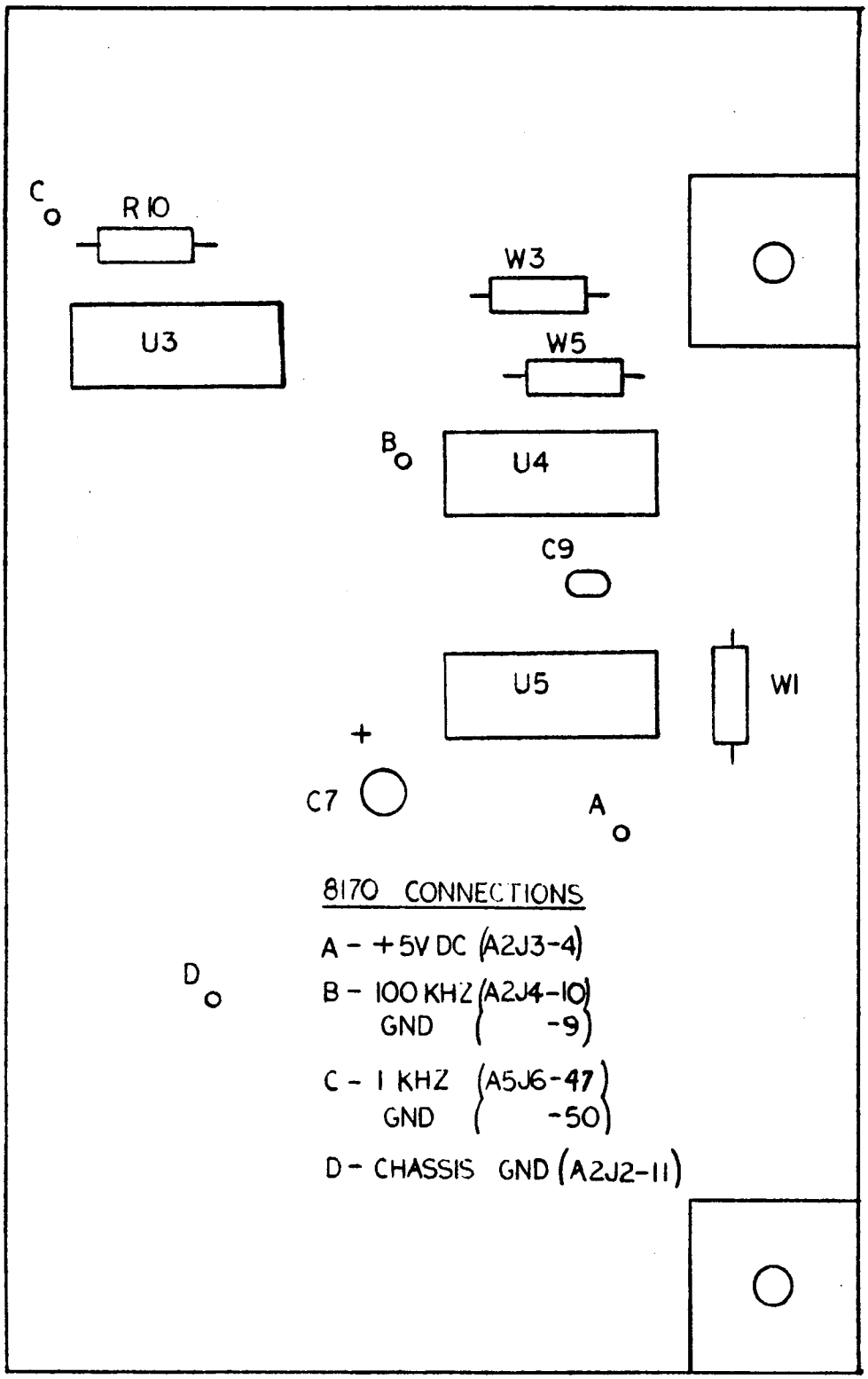


FIG. 4-10 OPTION 28 ASSEMBLY DRAWING

4.7.0 OPTION 30 - FULLY DECODED TEXT STREAM

The standard unit outputs serial ASCII day and time information via the 25-pin series D RS-232C connector and, if Option 19 is present, via the 9-pin series D RS-422 data connector.

The standard unit data stream gives the day of the year, 1-366. Option 30 outputs the day of the week, day of the month, month of the year and the last two digits of the year, i.e. FRI27FEB84.

The day-of-week and month is obtained algorithmically while the year data are read from two internal 10-position BCD switches. Switch A3SW3 sets the tens position of the year and A3SW1 sets the units position of year.

The algorithm that converts the day of the year to day-of-week and month-of-year is valid through the year 2010.

For details on the data structure, refer to Section 1.3.6 COMMANDS.

Option 30 data format is selected by placing switch A3SW4-2 in the ON position. To select the standard data format, place switch A3SW4-2 in the OFF position.

4.7.1 OPTION 30 - PRINCIPLES OF OPERATION

The Option 30 schematic is Figure 2-6, sheet 1. The assembly drawing is Figure 3-7.

Once per second the processor U12 converts the display day and time data from the standard format to the Option 30 format and adds the year information. The year data are read from switches A3SW1 and A3SW3. The Option 30 data is output on the RS-232C connector in response to a "T" command. See Section 1.3.6 COMMANDS for a des cription of the "T" command. If Option 19, Remote Output Driver is present, the Option 30 data stream is also fed out the Remote Output connector.

Switch A3SW4-2 Option 30 switch selects the standard data format if it is OPEN and the Option 30 format if it is CLOSED.

4.7.2 OPTION 30 - PERFORMANCE CHECKS

To verify the proper operation of Option 30, set the internal years switches A3SW1 (units) and A3SW3 (tens) to reflect the current year. Place switch A3SW4-2 in the ON position. Install the Model 8206 Antenna and obtain time synchronization. Connect an RS-232C terminal and obtain the time printout by depressing "T" on the key board. The printout will give the current day of the week, month, and year.

SECTION 5

PARTS LIST

ASSEMBLY	REF DESIG	PART NO	DESCRIPTION
Final Assembly	F1	F00R75	FUSE, 3/4A 3AG
Main Frame	A1	001100	RF Amplifier Assembly
	A2	001200-1	Receiver Assembly
	A3	014800	Microprocessor Assembly
	A4	014100	Display Assembly
	A5	014200	ption 24/25
Front Panel Ass'y	DS1	DS00042	Display, LED
	DS2,3	DS00045	''
Subchassis	T1	T10000	Transformer, Power
Rear Panel Ass'y	C1,2	C00202	Capacitor, .01 uf, 1.6
	J1	J00002	Receptacle, BNC, Crimp
	J2	J01000	Receptacle, AC Line
	J3,4	J00010	Receptacle, BNC
	S1	S00102	Switch, Slide, Double Pole
	S2	S00200	Nut Deco
		S00201	Switch, Toggle
	S3	S00300	Switch, Thumbwheel
	XF1	X00050	Fuseholder
		X00060	Fuseholder Cap
A1, RF Amplifier			
	C1	C07220	Capacitor, Electrolytic, 22 uf, 25V
	C2	C06182	Capacitor, Mica, 1800 pf
	C3	C09010	Capacitor, Electrolytic, 1 uf, 50V
	C4	C09010	Capacitor, Electrolytic, 1 uf, 50V
	C5	C09010	Capacitor, Electrolytic, 1 uf, 50V
	C6	C07220	Capacitor, Electrolytic, 22 uf, 25V
	C7	C05820	Capacitor, Mica, 82 pf
	C8	C00040	Capacitor, Trimmer, 4.5-20 pf
	C9	C00040	Capacitor, Trimmer, 4.5-20 pf
	C10	C05050	Capacitor, Mica, 5 pf
	C11	C09010	Capacitor, Electrolytic, 1 uf, 50V
	C12	C07220	Capacitor, Electrolytic, 22 uf, 25V
	C13	C09010	Capacitor, Electrolytic, 1 uf, 50V
	C14	C18103	Capacitor, Polystyrene, .01 uf
	C15	C18103	Capacitor, Polystyrene, .01 uf
	C16	C01104	Capacitor, Disc Ceramic, .1 uf
	C17	C09010	Capacitor, Electrolytic, 1 uf, 50V
	C18	C07220	Capacitor, Electrolytic, 22 uf, 25V
	C19	C09010	Capacitor, Electrolytic, 1 uf 50V
	C20	C09010	Capacitor, Electrolytic, 1 uf 50V
	C21	C09010	Capacitor, Electrolytic, 1 uf 50V
	C22	C07220	Capacitor, Electrolytic, 22 uf, 25V
	C23	C06182	Capacitor, Mica, 1800 pf

ASSEMBLY	REF DESIG	PART NO	DESCRIPTION
A1, RF Amplifier			
	L1	L03102	Choke, RF, 1000 uH
	L2	L03102	Choke, RF, 1000 uH
	L3	L03331	Choke, RF, 330 uH
	Q1	Q04126	Transistor, 2N4126
	Q2	Q04124	Transistor, 2N4124
	Q3	Q04124	Transistor, 2N4124
	R1	R01562	Resistor, 5.6K ohm, 1/4 W, 5%
	R2	R01273	Resistor, 27K ohm, 1/4 W, 5%
	R3	R01393	Resistor, 39K ohm, 1/4 W, 5%
	R4	R01183	Resistor, 18K ohm, 1/4 W, 5%
	R5	R01153	Resistor, 15K ohm, 1/4 W, 5%
	R6	R01152	Resistor, 1.5k ohm, 1/4 W, 5%
	R7	R01123	Resistor, 12K ohm, 1/4 W, 5%
	R8	R01332	Resistor, 3.3K ohm, 1/4 W, 5%
	R9	R01332	Resistor, 3.3K ohm, 1/4 W, 5%
	R10	R01332	Resistor, 3.3K ohm, 1/4 W, 5%
	R11	R01183	Resistor, 18K ohm, 1/4 W, 5%
	R12	R01183	Resistor, 18K ohm, 1/4 W, 5%
	R13	R01123	Resistor, 12K ohm, 1/4 W, 5%
	R14	R01683	Resistor, 68K ohm, 1/4 W, 5%
	R15	R01561	Resistor, 560 ohm, 1/4 W, 5%
	R16	R01681	Resistor, 680 ohm, 1/4 W, 5%
	R17	R01390	Resistor, 39K ohm, 1/4 W, 5%
	R18	R01100	Resistor, 10K ohm, 1/4 W, 5%
	R19	R05503	Potentiometer, 50K ohm
	R20	R01222	Resistor, 2.2K ohm 1/4 W, 5%
	S1	S00420	Switch, Slide, 2 Pole
	T1	T00020	Transformer
	U1	U01350	Integrated Circuit, MC1350P
	U2	U01350	Integrated Circuit, MC1350P
	Y1	Y00000	Crystal, Quartz, 60 kHz
A2, Receiver Assy.			
	C1	C01104	Capacitor, Disc Cer, 0.1 uf, 25 DCWV
	C2	C09010	Capacitor, Electrolytic, 1 uf, 50 DCWV
	C3	C01104	Capacitor, Disc Cer, 0.1 uf, 25 DCWV
	C4	C00100	Capacitor, Tant, CL65BE121MPE, 120 uf, 15 DCWV
	C5	C02103	Capacitor, Disc Cer, 0.01 uf, 50 DCWV
	C6	C07220	Capacitor, Electrolytic, 22 uf, 25 DCWV
	C7	C15685	Capacitor, Tant, 6.8 uf, 35 DCWV
	C8	C05560	Capacitor, Mica, 56 pf
	C9	C05200	Capacitor, Mica, 20 pf
	C10	C00040	Capacitor, Cer Trimmer, 4.5-20 pf
	C11	C05121	Capacitor, Mica, 120 pf

ASSEMBLY	REF DESIG	PART NO	DESCRIPTION
A2, Receiver Assy.			
	C12	C05301	Capacitor, Mica, 300 pf
	C13	C01104	Capacitor, Disc Cer, 0.1 uf, 25 DCWV
	C14	C18472	Capacitor, Polystyrene, 4700 pf, 160 DCWV
	C15	C18472	Capacitor, Polystyrene, 4700 pf, 160 DCWV
	C16	C09010	Capacitor, Electrolytic, 1.0 uf, 50 DCWV
	C17	C07220	Capacitor, Electrolytic, 22 uf, 25 DCWV
	C18	C07220	Capacitor, Electrolytic, 22 uf, 25 DCWV
	C19	C09010	Capacitor, Electrolytic, 1.0 uf, 50 DCWV
	C20	C01104	Capacitor, Disc Cer, 0.1 uf, 25 DCWV
	C21	C15105	Capacitor, Tant, 1.0 uf, 35 DCWV
	C22	C10157	Capacitor, Tant, 150 uf, 6 DCWV
	C23	C07220	Capacitor, Electrolytic, 22 uf, 25 DCWV
	C25	C02103	Capacitor, Disc Cer, 0.01 uf, 50 DCWV
	C26	C02103	Capacitor, Disc Cer, 0.01 uf, 50 DCWV
	C27	C02103	Capacitor, Disc Cer, 0.01 uf, 50 DCWV
	C28	C02103	Capacitor, Disc Cer, 0.01 uf, 50 DCWV
	C29	C02103	Capacitor, Disc Cer, 0.01 uf, 50 DCWV
	C44	C18392	Capacitor, Polystyrene, 3900 pf, 160 DCWV
	C45	C18751	Capacitor, Polystyrene, 750 pf, 160 DCWV
	C46	C18392	Capacitor, Polystyrene, 3900 pf, 160 DCWV
	C47	C07222	Capacitor, Electrolytic, 2200 uf, 25 DCWV
	C48	C07222	Capacitor, Electrolytic, 2200 uf, 25 DCWV
	C49	C07222	Capacitor, Electrolytic, 2200 uf, 25 DCWV
	C50	C07222	Capacitor, Electrolytic, 2200 uf, 25 DCWV
	C51	C09010	Capacitor, Electrolytic, 1.0 uf, 50 DCWV
	C52	C01104	Capacitor, Disc Cer, 0.1 uf, 50 DCWV
	C53	C08102	Capacitor, Electrolytic, 1,000 uf, 35 DCWV
	C54	C08102	Capacitor, Electrolytic, 1,000 uf, 35 DCWV
	C55	C09010	Capacitor, Electrolytic, 1.0 uf, 50 DCWV
	C56	C09010	Capacitor, Electrolytic, 1.0 uf, 50 DCWV
	C57	C01104	Capacitor, Disc Cer, 0.1 uf, 50 DCWV
	C58	C01104	Capacitor, Disc Cer, 0.1 uf, 50 DCWV
	C59	C09010	Capacitor, Electrolytic, 1.0 uf, 50 DCWV
	C60	C09010	Capacitor, Electrolytic, 1.0 uf, 50 DCWV
	CR1	CR04148	Diode, IN4148
	CR2	CR00209	Voltage Variable Capacitor, MV-209
	CR3	CR05059	Diode, IN5059
	CR4	CR04148	Diode, IN4148
	CR9	CR05624	Diode, IN5624
	CR11	CR05624	Diode, IN5624
	CR12	CR05059	Diode, IN5059
	CR13	CR05059	Diode, IN5059
	CR14	CR05059	Diode, IN5059
	CR15	CR05059	Diode, IN5059
	CR16	CR04148	Diode, IN4148

ASSEMBLY	REF DESIG	PART NO	DESCRIPTION
A2, Receiver Assy.			
	E1	E02320	Terminal, Turret
	E2	E02320	Terminal, Turret
	E3	E02320	Terminal, Turret
	E4	E02320	Terminal, Turret
	J1	J10014	Receptacle, 6 pins
	J2	J10014	Receptacle, 6 pins
	J3	J10014	Receptacle, 6 pins
	J4	J10014	Receptacle, 6 pins
	J5	J10014	Receptacle, 6 pins
	L1	L03152	Choke, 1500 uH
	L2	L03152	Choke, 1500 uH
	L3	L03152	Choke, 1500 uH
	Q1	Q04126	Transistor, 2N4126
	Q2	Q04126	Transistor, 2N4126
	Q3	Q04124	Transistor, 2N4124
	Q4	Q04258	Transistor, 2N4258
	Q5	Q04126	Transistor, 2N4126
	Q9	Q04124	Transistor, 2N4124
	R1	R01471	Resistor, 1/4 W, 5%, 470 ohms
	R2	R01561	Resistor, 1/4 W, 5%, 560 ohms
	R3	R01561	Resistor, 1/4 W, 5%, 560 ohms
	R4	R01472	Resistor, 1/4 W, 5%, 4.7K ohms
	R5	R05202	Potentiometer, Trimming, Cermet, 2K ohms
	R6	R21512	Resistor, Metal Glaze, 1/4 W, 2%, 5.1K ohms
	R7	R21562	Resistor, Metal Glaze, 1/4 W, 2%, 5.6K ohms
	R8	R21562	Resistor, Metal Glaze, 1/4 W, 2%, 5.6K ohms
	R9	R01393	Resistor, 1/4 W, 5%, 39K ohms
	R10	R01393	Resistor, 1/4 W, 5%, 39K ohms
	R11	R01104	Resistor, 1/4 W, 5%, 100K ohms
	R12	R01102	Resistor, 1/4 W, 5%, 1K ohms
	R13	R01472	Resistor, 1/4 W, 5%, 4.7K ohms
	R14	R05502	Potentiometer, Trimming, Cermet, 5K ohms
	R15	R01272	Resistor, 1/4 W, 5%, 2.7K ohms
	R16	R01562	Resistor, 1/4 W, 5%, 5.6K ohms
	R17	R01562	Resistor, 1/4 W, 5%, 5.6K ohms
	R18	R01104	Resistor, 1/4 W, 5%, 100K ohms
	R19	R01393	Resistor, 1/4 W, 5%, 39K ohms
	R20	R01153	Resistor, 1/4 W, 5%, 15K ohms
	R21	R01332	Resistor, 1/4 W, 5%, 3.3K ohms
	R22	R01330	Resistor, 1/4 W, 5%, 33 ohms
	R23	R05102	Potentiometer, Trimming, Cermet, 1K ohms
	R24	R01331	Resistor, 1/4 W, 5%, 330 ohms
	R25	R01471	Resistor, 1/4 W, 5%, 470 ohms
	R26	R01561	Resistor, 1/4 W, 5%, 560 ohms
	R27	R01561	Resistor, 1/4 W, 5%, 560 ohms
	R28	R01472	Resistor, 1/4 W, 5%, 4.7K ohms
	R29	R01152	Resistor, 1/4 W, 5%, 1.5K ohms

ASSEMBLY	REF DESIG	PART NO	DESCRIPTION
A2, Receiver Assy.			
	R30	R05202	Potentiometer, Trimming, Cermet, 2K ohms
	R31	R21512	Resistor, Metal Glaze, 1/4 W, 2%, 5.1K ohms
	R32	R21562	Resistor, Metal Glaze, 1/4 W, 2%, 5.6K ohms
	R33	R21562	Resistor, Metal Glaze, 1/4 W, 2%, 5.6K ohms
	R34	R01472	Resistor, 1/4 W, 5%, 4.7K ohms
	R35	R01332	Resistor, 1/4 W, 5%, 3.3K ohms
	R36	R01153	Resistor, 1/4 W, 5%, 15K ohms
	R37	R01153	Resistor, 1/4 W, 5%, 15K ohms
	R38	R21154	Resistor, Metal Glaze, 1/4 W, 2%, 150K ohms
	R39	R21153	Resistor, Metal Glaze, 1/4 W, 2%, 15K ohms
	R40	R21154	Resistor, Metal Glaze, 1/4 W, 2%, 150K ohms
	R42	R01153	Resistor, 1/4 W, 5%, 15K ohms
	R43	R01475	Resistor, 1/4 W, 5%, 4.7 Megohms
	R44	R01332	Resistor, 1/4 W, 5%, 3.3K ohms
	R45	R01473	Resistor, 1/4 W, 5%, 47K ohms
	R46	R01563	Resistor, 1/4 W, 5%, 56K ohms
	R47	R01394	Resistor, 1/4 W, 5%, 390K ohms
	R48	R01105	Resistor, 1/4 W, 5%, 1 Megohms
	R49	R01332	Resistor, 1/4 W, 5%, 3.3K ohms
	R50	R01221	Resistor, 1/4 W, 5%, 220 ohms
	R51	R01103	Resistor, 1/4 W, 5%, 10K ohms
	R52	R01103	Resistor, 1/4 W, 5%, 10K ohms
	R53	R01151	Resistor, 1/4 W, 5%, 150 ohms
	R54	R01332	Resistor, 1/4 W, 5%, 3.3K ohms
	R55	R01560	Resistor, 1/4 W, 5%, 56 ohms
	R56	R01560	Resistor, 1/4 W, 5%, 56 ohms
	R83	R01272	Resistor, 1/4 W, 5%, 2.7K ohms
	R85	R01682	Resistor, 1/4 W, 5%, 6.8K ohms
	R86	R01182	Resistor, 1/4 W, 5%, 1.8K ohms
	R87	R01101	Resistor, 1/4 W, 5%, 100 ohms
	R88	R01152	Resistor, 1/4 W, 5%, 1.5K ohms
	R89	R21153	Resistor, Metal Glaze, 1/4 W, 2%, 15K ohms
	TP1	TP00001	Test Point, Brown
	TP2	TP00002	Test Point, Red
	TP3	TP00003	Test Point, Orange
	TP4	TP00004	Test Point, Yellow
	TP6	TP00006	Test Point, Blue
	U1	U01496	Integrated Circuit, LM1496N
	U2	U00324	Integrated Circuit, LM324N
	U3	U01496	Integrated Circuit, LM1496N
	U4	U00339	Integrated Circuit, LM339N
	U5	U4LS37	Integrated Circuit, SN74LS37
	U6	U4S140	Integrated Circuit, SN74S140N
	U7	U4LS37	Integrated Circuit, SN74LS37
	U8	U4LS90	Integrated Circuit, SN74LS90
	U9	U4LS90	Integrated Circuit, SN74LS90
	U10	U4LS90	Integrated Circuit, SN74LS90

ASSEMBLY	REF DESIG	PART NO	DESCRIPTION
A2, Receiver Assy.			
	U16	U4LS90	Integrated Circuit, SN74LS90
	U21	U07805	Voltage Regulator, 7805UC
	U22	U78M12	Voltage Regulator, 78M12UC
	U23	U79M12	Voltage Regulator, 79M12AUC
	VR2	VR04735	Zener Diode, IN4735A
	W1	R01000	Jumper
	W2	R01000	Jumper
	W3	R01000	Jumper
	Y1	Y00011	Crystal, Quartz
8170 Microprocessor			
	U1	U08155	Integrated Circuit 8155
	U2	U08155	Integrated Circuit 8155
	U3	U08755	Integrated Circuit 8755A
	U4	U08255	Integrated Circuit 8255A (Opt. 18)
	U5	U08755	Integrated Circuit 8755A
	U6	U08755	Integrated Circuit 8755A (Opt. 23)
	U7	ULS109	Integrated Circuit 74LS109
	U8	U4LS90	Integrated Circuit 74LS90
	U9	U08251	Integrated Circuit 8251A
	U10	U08251	Integrated Circuit 8251A
	U11	U08259	Integrated Circuit 8259A
	U12	U08085	Integrated Circuit 8085A
	U13	U4S140	Integrated Circuit 74S140 (Opt. 23)
	U14	U08253	Integrated Circuit 8253-5
	U15	U08253	Integrated Circuit 8253-5
	U16	U08253	Integrated Circuit 8253-5 (Opt. 23)
	U17	U08253	Integrated Circuit 8253-5 (Opt. 23)
	U18	U00324	Integrated Circuit LM324 (Opt. 23)
	U19	U01488	Integrated Circuit MC1488
	U20	U4LS04	Integrated Circuit 74LS04
	U21	ULS423	Integrated Circuit 74LS423
	U22	U4LS02	Integrated Circuit 74LS02
	U23	ULS138	Integrated Circuit 74LS138
	U24	U00555	Integrated Circuit NE555
	U25	UC4053	Integrated Circuit CD4053B (Opt. 23)
	U26	U01489	Integrated Circuit MC1489A
	U27	U4S140	Integrated Circuit 74S140
	U28	U0MF10	Integrated Circuit MF10 (Opt. 23)
	U29	U6LS31	Integrated Circuit AM26LS31
	U30	ULS138	Integrated Circuit 74LS138 (Opt. 18)
	C1	C26104	Capacitor, Disc, 0.1 uf, 25V
	C2	C26104	Capacitor, Disc, 0.1 uf, 25V
	C3	C26104	Capacitor, Disc, 0.1 uf, 25V

ASSEMBLY	REF DESIG	PART NO	DESCRIPTION
8170 Microprocessor			
	C4	C26104	Capacitor, Disc, 0.1 uf, 25V
	C5	C26104	Capacitor, Disc, 0.1 uf, 25V
	C6	C26104	Capacitor, Disc, 0.1 uf, 25V
	C7	C26104	Capacitor, Disc, 0.1 uf, 25V
	C8	C26104	Capacitor, Disc, 0.1 uf, 25V
	C9	C26104	Capacitor, Disc, 0.1 uf, 25V
	C10	C26104	Capacitor, Disc, 0.1 uf, 25V
	C11	C26104	Capacitor, Disc, 0.1 uf, 25V
	C12	C26104	Capacitor, Disc, 0.1 uf, 25V
	C15	C26104	Capacitor, Disc, 0.1 uf, 25V
	C16	C26104	Capacitor, Disc, 0.1 uf, 25V
	C17	C07220	Capacitor, Electrolytic, 22 uf, 25V
	C18	C26104	Capacitor, Disc, 0.1 uf, 25V
	C19	C26104	Capacitor, Disc, 0.1 uf, 25V
	C20	C05301	Capacitor, Mica, 300 pf
	C21	C05301	Capacitor, Mica, 300 pf
	C22	C05560	Capacitor, Mica, 56 pf (Opt. 23)
	C23	C07220	Capacitor, Electrolytic, 22 uf, 25V
	C24	C07220	Capacitor, Electrolytic, 22 uf, 25V
	C25	C15105	Capacitor, Electrolytic, 1 uf 35V (Opt. 23)
	C26	C26104	Capacitor, Disc, 0.1 uf, 50V
	C27	C26104	Capacitor, Disc, 0.1 uf, 50V
	C28	C09101	Capacitor, Electrolytic, 1 uf, 50V
	CR2	CR00277	Diode 6E, IN277
	CR3	CR00277	Diode 6E, IN277
	CR4	CR00277	Diode 6E, IN277
	R1	R01103	Resistor, 1/4 W, 5%, 10K (Opt. 30)
	R2	R01103	Resistor, 1/4 W, 5%, 10K
	R3	R01103	Resistor, 1/4 W, 5%, 10K
	R4	R01472	Resistor, 1/4 W, 5%, 4.7K
	R5	R01103	Resistor, 1/4 W, 5%, 10K
	R6	R01151	Resistor, 1/4 W, 5%, 150
	R7	R01512	Resistor, 1/4 W, 5%, 5.1K
	R8	R01102	Resistor, 1/4 W, 5%, 1K (Opt. 23)
	R9	R01102	Resistor, 1/4 W, 5%, 1K (Opt. 23)
	R10	R01103	Resistor, 1/4 W, 5%, 10K
	R11	R01103	Resistor, 1/4 W, 5%, 10K
	R12	R01103	Resistor, 1/4 W, 5%, 10K
	R13	R01361	Resistor, 1/4 W, 5%, 360 (Opt. 23)
	R14	R01223	Resistor, 1/4 W, 5%, 22K (Opt. 23)
	R15	R01510	Resistor, 1/4 W, 5%, 51 (Opt. 23)
	R16	R01103	Resistor, 1/4 W, 5%, 10K
	R17	R01103	Resistor, 1/4 W, 5%, 10K (Opt. 23)
	R18	R01224	Resistor, 1/4 W, 5%, 220K

ASSEMBLY	REF DESIG	PART NO	DESCRIPTION
8170 Microprocessor			
	R19	R01122	Resistor, 1/4 W, 5%, 1.2K
	R20	R01104	Resistor, 1/4 W, 5%, 100K
	R21	R01333	Resistor, 1/4 W, 5%, 33K (Opt. 23)
	R22	R01103	Resistor, 1/4 W, 5%, 10K (Opt. 23)
	R23	R01183	Resistor, 1/4 W, 5%, 18K (Opt. 23)
	R24	R01103	Resistor, 1/4 W, 5%, 10K
	R25	R01103	Resistor, 1/4 W, 5%, 10K (Opt. 23)
	R26	R01103	Resistor, 1/4 W, 5%, 10K (Opt. 23)
	R27	R01103	Resistor, 1/4 W, 5%, 10K (Opt. 23)
	R28	R01103	Resistor, 1/4 W, 5%, 10K (Opt. 23)
	R29	R01103	Resistor, 1/4 W, 5%, 10K (Opt. 23)
	R30	R01472	Resistor, 1/4 W, 5%, 4.7K (Opt. 23)
	R31	R01121	Resistor, 1/4 W, 5%, 120
	R32	R01121	Resistor, 1/4 W, 5%, 120
	R33	R01121	Resistor, 1/4 W, 5%, 120
	R34	R01121	Resistor, 1/4 W, 5%, 120
	R35	R01121	Resistor, 1/4 W, 5%, 120
	R36	R01102	Resistor, 1/4 W, 5%, 1K
	R37	R01102	Resistor, 1/4 W, 5%, 1K
	R38	R01102	Resistor, 1/4 W, 5%, 1K
	R39	R01104	Resistor, 1/4 W, 5%, 100K
	J1	J02020	Receptacle, 20 pin
	J2	J03213	Receptacle, 26 pin
	J3	J03213	Receptacle, 26 pin
	J4	J02225	Receptacle, 50 pin
	J5	J03213	Receptacle, 26 pin
	J6	J02020	Receptacle, 20 pin
	SW1	S00320	1 Pole, 10 Pos (Opt. 30)
	SW2	S00320	1 Pole, 10 Pos
	SW3	S00320	1 Pole, 10 Pos (Opt. 30)
	SW4	S00332	Dip Switch, 4 SPST
	SW5	S00320	1 Pole, 10 Pos (Opt. 23)
	SW6	S00340	Dip Switch, 1 SPST (Opt. 23)
	VR1	VR04733	Zener Diode, IN4733A (Opt. 23)
	Y1	Y00012	Crystal, 6.144 MHz
	Q1	Q04124	Transistor, 2N4124
	RP1	R36103	Resistor 7-10K
	RP2	R36103	Resistor 7-10K
	RP3	R36103	Resistor 7-10K
	RP4	R36103	Resistor 7-10K (Opt. 30)
	RP5	R36103	Resistor 7-10K (Opt. 18, 23)

ASSEMBLY	REF DESIG	PART NO	DESCRIPTION
A4, Display			
	C1	C01104	Capacitor, Disc 0.1 uf, 25V
	DS1,2	DS00052	Display, L.E.D.
	J1	J03213	Receptacle, 6 pin
	R1,2	R01330	Resistor Metal, 1/4 W, 5%, 33 ohms
	U1-4	DS00072	Display, L.E.D.
	U5,6	DS00012	Display, L.E.D.
	U7	U7218C	Display Driver
Option 15			
	C1	C02103	Capacitor, Disc, .01 uf, 25V
	C2	C18392	Capacitor, Poly, 3900 uf
	C3	C18751	Capacitor, Poly, 750 uf
	C4	C18392	Capacitor, Poly, 3900 uf
	C5-8	C02103	Capacitor, Disc, .01 uf, 25V
	C9	C01104	Capacitor, Disc, .1 uf, 25V
	C10	C07220	Capacitor, Elect, 22 uf, 25V
	C11,12	C01100	Capacitor, Disc, .1 uf, 25V
	C13-15	C07220	Capacitor, Elect, 22 uf, 25V
	CR1	CR04148	Diode, IN4148
	L1,2	L03152	Choke, 1500 uH
	Q1	Q04124	Transistor 2N4124
	Q2	Q04258	Transistor 2N4258
	Q5	Q04258	Transistor 2N4258
	R1	R01272	Resistor, 1/4 W, 5%, 2.7K
	R2	R01682	Resistor, 1/4 W, 5%, 6.8K
	R3	R01182	Resistor, 1/4 W, 5%, 1.8K
	R4	R01682	Resistor, 1/4 W, 5%, 6.8K
	R5,6	R01472	Resistor, 1/4 W, 5%, 4.7K
	R7	R01102	Resistor, 1/4 W, 5%, 1K
	R8,9	R01272	Resistor, 1/4 W, 5%, 2.7K
	R10,11	R01560	Resistor, 1/4 W, 5%, 560 ohms
	U1-4	U4LS90	Integrated Ckt, SN75LS90
	U5	U4LS92	Integrated Ckt, SN74LS92
	U6	U4LS90	Integrated Ckt, SN74LS90
	U7	U4S140	Integrated Ckt, SN74LS140
	U10	ULS132	Integrated Ckt, SN74LS132
Option 24/25			
	C1	C26104	Capacitor, Disc, 0.1 uf, 50V
	C2,3	C07220	Capacitor, Elect, 22 uf, 25V
	C4-6	C26104	Capacitor, Disc, 0.1 uf, 50V
	C7	C09010	Capacitor, Elect, 1 uf, 50V
	CR1	CR00277	Diode, IN277
	J1	J02020	Receptacle, 20 pins
	R1	R01102	Resistor, 1/4 W, 5%, 1K
	R2	R01000	Jumper
	R3	R01101	Resistor, 1/4 W, 5%, 100
	R4	R01102	Resistor, 1/4 W, 5%, 1K

ASSEMBLY	REF DESIG	PART NO	DESCRIPTION
Option 24/25			
	U1	U4LS90	Integrated Ckt, SN74LS90
	U2	ULS151	Integrated Ckt, SN74LS151
	U3	U75175	Integrated Ckt, SN75175
	U4	U4S132	Integrated Ckt, SN74S132
	U5	014305	Oscillator, TCXO 1 MHz (Op.24 only)
Option 28			
	C7	C07270	Capacitor, Elect, 22 uf, 25v
	C9	C02103	Capacitor, Disc, 0.01 uf
	R10	R01560	Resistor, 1/4 W, 5%, 56 ohm
	U3	U4LS140	Integrated Ckt, SN74LS140
	U4,5	U4LS90	Integrated Ckt, SN74LS90

THE FOLLOWING IS A LIST OF MANUAL REVISIONS

PAGE	DATE	REVISION
ALL	10/05/89 ECN 171	Due to popular demand, Option 30 Fully Decoded Text Stream has been made standard. This feature has been added to all model 8170s with serial numbers 8170-0766 and above. The receiver is sent from the factory with the Fully Decoded Text Stream enabled. If the alternate data stream is required, place SW4-2 in the OFF position. Throughout the manual, the Fully Decoded Text Stream output maintains the Option 30 identifier.
1 - 10	01/16/89 ECN 143	The Option 30 year switches have been relocated to the rear panel for customer convenience. The switches are mounted in the parallel BCD cut out unless the unit is equipped with that option, then the switches will be on the microprocessor board. Add the following to section 1.3.2 Rear Panel Functions. TENS UNITS YEAR SWITCHES: these are the year switches used in the Option 30 Fully Decoded Text Stream. Set switches to the current year.
1 - 12	01/16/89 ECN 143	The Option 30 year switches have been relocated to the rear panel for customer convenience. Only if the unit is equipped with Option 18, Parallel BCD Output, do the switches remain internal.
1 - 14, 4 - 10	01/16/89 ECN 140	Option 30 Fully Decoded Text Stream data format has been changed to the following: (CR)(LF) I X WWW (SPACE) DDMMMYY (SPACE) HH:MM:SS (CR)(LF) Where: I = SPACE if clock is synchronized to WWVB * if clock is manually set by RS-232 port ? if time sync lamp is off X = SPACE if current year agrees with Option 30 year switch setting $ if current year does not agree with Option 30 year switch setting WWW = Day of Week (Mon, Tue, Wed, etc.) DD = Numeric Day of Month (01 to 31) MMM = Month (Jan, Feb, Mar, etc.) YY = Year (89, 90, 91 etc.) HH:MM:SS = Hours:Minutes:Seconds (CR) and (LF) are ASCII control characters

1 - 15 06/19/89 ECN 153

Insert the following errata into Section 1.3.6 COMMANDS.

"Y" Command - This command allows the Option 30 year data to be set via the RS-232 port. To set the year, enter the following into the serial ASCII port:

YAB

Where: Y = capital letter Y. Typing this initializes the year set command.

A = tens of years

B = units of years

Example: To set the year 1989, enter Y89.

Do not type ENTER or RETURN to terminate the command.

The "Y" command will only be accepted by the clock when in the Option 30 Fully Decoded Text Stream, mode (SW4-2 ON).

4 - 30 ECN 140 ECN 153

Replace section 4.7.0, 4.7.1 & 4.7.2 Option 30 Fully Decoded Text Stream with the following:

4.7.0 OPTION 30 - FULLY DECODED TEXT STREAM

Option 30 converts the day of the year, 1-366, into day of the week, day of the month, month of the year and the last two digits of the year, i.e. MON 16 JAN 89.

The complete Option 30 data structure is shown below.

(CR)(LF) I X WWW (SPACE) DDMMMYY (SPACE) HH:MM:SS (CR)(LF)

Where: I = SPACE if clock is synchronized to WWVB
* if clock is manually set by RS-232 port
? if time sync lamp is off

X = SPACE if current year agrees with Option 30 year switch setting

$ if current year does not agree with Option 30 year switch setting

WWW = Day of Week (Mon, Tue, Wed, etc.)
DD = Numeric Day of Month (01 to 31)
MMM = Month (Jan, Feb, Mar, etc.)
YY = Year (89, 90, 91 etc.)
HH:MM:SS = Hours:Minutes:Seconds

(CR) and (LF) are ASCII control characters

The day of week and month is obtained algorithmically, while the year data is obtained from two 10-position BCD switches. These switches are found on the rear panel unless the unit is equipped with Option 18, Parallel BCD. Then, the switches are located on the microprocessor board. Switch SW3 sets the tens of years and switch SW1 sets the years units.

The year data may also be entered into the clock by using the "Y" command. To set the year, enter the following into the serial ASCII port:

YAB

Where: Y = capital letter Y. Typing this initializes the year set command.

A = tens of years

B = units of years

Example: To set the year 1989, enter Y89.

Do not type ENTER or RETURN to terminate the command.

The clock will automatically increment to the new year at midnight New Years Eve. A "$" will appear in the data stream to indicate that the year switch settings do not coincide with the year being output on the data stream. The "$" is removed from the data stream when the year switches are set to the current year or the year setting entered by a "Y" command.

NOTE: The year variable entered with a "Y" command or the result of the automatic end-of-year rollover, is stored in volatile RAM. If a power outage occurs, the clock will read the year switch settings at power up and will output the date relative to the switch settings.

The algorithm that converts day of the year to day of the week and month of year is valid through the year 2019.

The Option 30 format is output to both the RS-232 and RS-422 ports whenever switch SW 4-2 is in the ON position. To select the standard format, place switch SW 4-2 in the OFF position.